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FUNDAMENTAL ISSUES IN SPACE ELECTRONICS RELIABILITY: NEGATIVE BIAS TEMPERATURE INSTABILITY

BY

JESSE K. MEE

BACHELOR'S OF SCIENCE

THESIS

Submitted in Partial Fulfillment of the
Requirements for the Degree of

Master of Science

Electrical Engineering

The University of New Mexico
Albuquerque, New Mexico

December, 2010

DEDICATION

I dedicate this work to my wife Hannah, my son Trevor, and my daughter Lillian. My academic achievements would be meaningless without the love and support of my family.

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I would first and foremost like to acknowledge to the extraordinary effort of Dr. Rod Devine for his assistance with experimental development, and conceptual understanding. None of this work would have been possible without his guidance. I would like to give a special thanks to Dr. Len Trombetta, Dr. Robert Kaplar, Dr. Harry Hjalmarson, and Dr. P. Goukar for their support of this research. I would like to thank Mr. Marc Owens for giving me the facility and the resources to perform this research. I would like to thank my friends and family for their love and support. I would finally like to thank my thesis committee members; Dr. Luke Lester, Dr. Rod Devine, and Dr. Olga Lavrova.

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by

Jesse K. Mee

B.S., Electrical Engineering, University of New Mexico, 2009
M.S., Electrical Engineering, University of New Mexico, 2010

ABSTRACT

Negative Bias Temperature Instability (NBTI) in silicon based metal-oxide-semiconductor-field-effect-transistors (MOSFETs) has been recognized as a critical reliability issue for advanced space qualified electronics. The phenomenon manifests itself as a modification of threshold voltage (V_{th}) resulting in degraded signal timing paths, and ultimately circuit failure. Despite the obvious importance of the issue, a standard measurement protocol has yet to be determined. This is a consequence of a large amount of complexity introduced by the strong dependencies of NBTI on temperature, electric field, frequency, duty cycle, and gate dielectric composition. Indeed, researchers are nowhere near a dependable circuit reliability lifetime predictor formula that would be accurate among a wide variety of technology specifications.

We have improved upon the traditional measurement techniques which suffered from an underestimation of the magnitude of V_{th} shifts because they failed to account for trapped charge relaxation. Specifically, we have developed a means for measuring the

maximum effect of NBTI by virtue of a method that can continuously monitor the $V_{th}(t)$ without having to remove the stressing voltage. The interpretation methodology for this technique is explained in detail and the relevant approximations are justified. Using this method, we have examined the time and magnitude dependencies of change in V_{th} as a function of time ($\Delta V_{th}(t)$) on temperature, vertical electric field, inversion channel carrier density, and source-drain voltage (V_{ds}).

In the work presented here, we have evidenced temperature and vertical electric field dependent V_{th} shifts in SiO_2 and HfSiON devices. Furthermore, we have collected substantial evidence that the traditional $\Delta V_{th}=At^{\alpha}$ analysis fails to explain the experimental data in the early time domain. Finally, we have discovered that $\Delta V_{th}(t)$ on p-channel field effect transistors with HfSiON gate dielectrics is dependent upon the magnitude of V_{ds} during the stressing cycle. To our knowledge this is not anticipated by any prior modeling attempts. We justify the exclusion of short channel effects as a possibility, leading us to conclude that positive charge in the dielectric stack is laterally mobile and subsequently transported out of the dielectric in the presence of the lateral electric field induced by V_{ds}.

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1. Chapter 1 – Introduction

1.1 Background

It is well known that silicon based technology for radiation hardened space electronics is several technology generations behind its commercial counterparts; this is illustrated in FIG 1-1. So while presently hardened devices in the 90 – 65 nm node are in the research and development phase, commercial industry is addressing the developmental issues relating to 22 nm devices. A positive consequence of this delay is that the reliability lifetime, a current problem in the commercial industry, has not yet impacted the world of space based electronics.

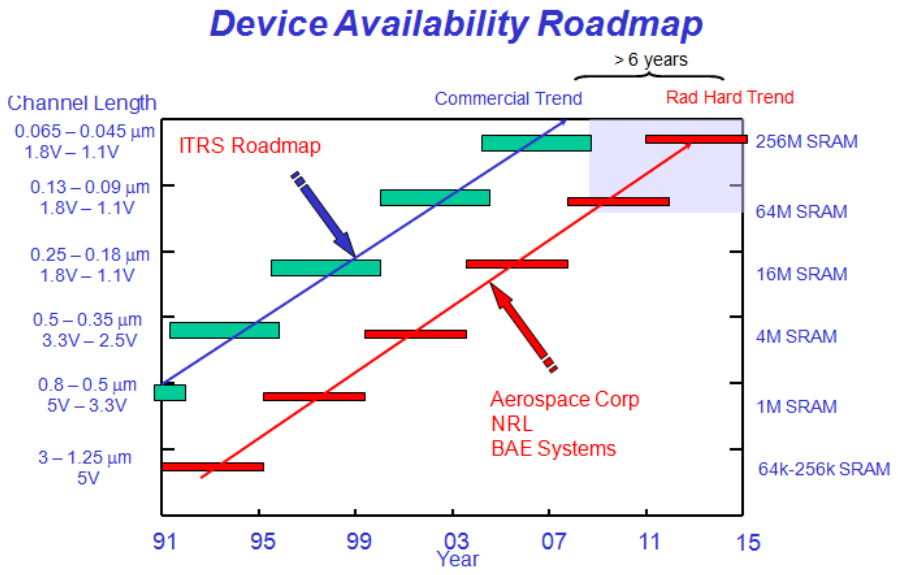

Figure 1-1 Device Availability Roadmap comparing the radiation hard trend to the commercial trend

As silicon based technology evolves, increased device performance is being achieved by both scaling of transistor feature sizes and also by the introduction of new materials

whose influence on device reliability may be relatively unknown. In the former case the scaling of gate oxide thicknesses below 2nm without the corresponding reduction in supply voltage resulted in increased oxide electric fields and enhanced leakage currents. Compounded with the rapid increase in new materials and inherent risk of reliability loss, scaling results in increased power dissipation resulting from the density of active devices in a given chip area. Power dissipation is well known [1] to result in increased operational temperatures leading to more rapid deviation of device characteristics (threshold voltage shift, carrier mobility,…) and interconnect failure due to mechanisms such as electromigration. In the case of temperature enhanced device characteristic variation, one of the prime mechanisms in metal-oxide-semiconductor field effect transistor (MOSFET) p-channel devices is the *negative bias temperature instability (NBTI)*. Various authors have suggested that this degradation mechanism may be dominant in advanced, strongly-sub-micronic technology. In addition, an equivalent effect in n-channel MOSFET devices has been observed and termed *positive bias temperature instability (PBTI)* which results from elevated temperature and positive bias with respect to substrate. It has been repeatedly shown, however, that characteristic shifts due to PBTI are significantly less than the shifts observed in NBTI. As a result, it is widely accepted that the underlying physical mechanism behind the phenomenon of NBTI results in the generation and trapping of positive charge. The origin of this positive charge remains in question and has captured the interest of researchers all over the world.

From perspective of circuit lifetime, PBTI and NBTI result in asymmetric degradation of the n-channel and p-channel MOSFETs since in magnitude NBTI>PBTI so to speak. The asymmetry induced generates timing issues that can ultimately lead to

logic upsets. This is evident by analysis of the full square law model for source drain current in a MOSFET [2],

$$I_{ds} = (W/L)\, \mu_{eff} C_{ox} [\{V_{gs} - (V_{th}^{o} + \Delta V_{th})\} V_{ds} - 1/2 V_{ds}^{2}] \qquad (1\text{-}1)$$

where W is the channel width, L the channel length and C_{ox} the gate dielectric stack capacitance. μ_{eff} is the effective mobility of the inversion channel carriers (holes or electrons). In the p-channel devices, positive charge is trapped somewhere in the gate dielectric effectively making the threshold voltage (V_{th}) more negative. From Eq. 1-1, an increase in $|(V_{th} + \Delta V_{th})|$ will result in a decrease in I_{ds} for a given V_{gs}. Coupled with the fact that the delay time for signal arrival in a CMOS circuit is inversely proportional to the source-drain current (I_{ds}) of the transistor, the effect of NBTI will be to increase the delay time. As for the n-channel devices, the V_{th} remains essentially constant and thus an increased spread in signal arrival times is created. This degradation of the timing paths can potentially lead to logic upsets and ultimately circuit failure.

In the light of the previous discussion one might have expected that evidence of a reliability lifetime issue due to such mechanisms as NBTI in advanced CMOS technology would have already had a significant negative impact on the commercial industry. However, it has not and the explanation for this revolves around two characteristics of the commercial industry. The first is that commercial products are increasingly replaced after a few years of use (i.e. before wear-out) and thus strict lifetime requirements such as the old 24/7 for 10 years are not necessary. Secondly, the worst case, continuous operation scenario is seldom observed in modern electronics and one must consider, for example,

the duty cycle which can dramatically reduce the device "on time". Given that the characteristics of observed trapped charge relaxation phenomena occurring in NBTI [3], one can conclude that nature fortuitously works in reducing the overall magnitude of degradation. As an example, tests on 65 nm technology produced by one of the world"s premier manufacturers of microelectronics (TSMC) resulted in a DC lifetime of 0.2 years and an AC lifetime of 10 years [4]! However, the reliability of advanced CMOS technology is a major cause for concern in the space industry where certain satellite applications require operational lifetimes ~ 10 – 15 years. Among the various mechanisms contributing to reliability loss in satellite electronics, such as electronic reliability (NBTI and PBTI), and the effects of irradiation via total ionizing dose and/or single event upset, NBTI is the least understood and continues to generate the most concern. It is crucial that a deeper understanding of the origin and nature of NBTI be achieved. The space industry will clearly evolve to more advanced technologies and device reliability will become the primary factor limiting the lifetime of a satellite.

Although the origin of NBTI is not understood, it appears clear that it is intimately related to the physics of the gate insulator/semiconductor interface and certainly, increasingly, to the nature of the complex oxide used as the gate insulator. In more advanced fabrication processes higher dielectric constant (κ) gate insulators are being introduced in order to enable thicker dielectric films to be employed. Note that to first order the leakage current varies inverse exponentially with the dielectric thickness (t_{ox}) [5] and that the gate capacitance $C \propto \kappa/t_{ox}$. Consequently, the same gate capacitance can be achieved using higher κ films which are thicker. However, it has been observed experimentally the use of high-κ films enhanced NBTI and consequently

degraded lifetime reliability results. In the simplest case, this is believed to be the result from increased charge trap density in complex oxides. However, the real picture becomes much more complicated when we consider the process steps involved in the creation of the gate stack. First one starts with a thin (~ 1 nm) SiO_2 layer on the Si substrate, this is followed by an alternative dielectric such as HfSiO which may be then nitrided to form HfSiON. This process will not result in a simple HfSiON/Si gate stack but more likely at the very least HfSiON/SiON/Si having a minimum of two relevant mismatch interfaces (HfSiON/SiON and SiON/Si) and two "bulk" dielectrics, HfSiON and SiON, with their own charge trapping defect sites. The resulting complexity of the gate stack presently prevents identification of the exact nature and location of the traps and/or their spatial distribution. On the other hand, comparing the charging and relaxation kinetics of a device with a simple SiO_2 gate dielectric to a device with a "high κ" gate dielectric can offer valuable insight into the physical mechanism of NBTI.

Perhaps one of the most challenging aspects in the study of NBTI is the fact that measurement techniques vary considerably from one research group to another making cross referencing of research results very difficult. Though it appears unlikely at the present time, ultimately a generic protocol for the measurement of stress induced threshold voltage degradation needs to be established. As we will discuss in detail, in our own approach we target the reduction of error resulting from trapped charge relaxation by sustaining the stress throughout the experiment. This is achieved by measuring the change in source-drain current with time $I_{ds}(t)$ while maintaining a stressing voltage on the gate and drain contacts. The device threshold voltage shift ΔV_{th} can then be extracted from the fractional current change I_{ds}/I_{ds}^{o}. Bearing in mind certain approximations which

we will validate in a later chapter, the result of this continuous stress measurement will be shown to be a good representation of the full effect of trapped charge on the threshold voltage **in the DC stress mode**. This proves to be a crucial piece of information when trying to develop a better understanding of the physics, but may not be the best method on which to base a reliability lifetime predictor model. Building a reliable lifetime predictor formula will require careful examination of the circuit operation conditions as well as technology specifications.

1.2 Experimental Objective

On the basis of the above discussion we developed a set of objectives for this thesis. Initially we will familiarize our self with optimized measurement techniques and data interpretation methodology for NBTI lifetime assessment. Upon development of optimized experimental procedures, we will study NBTI in advanced high-κ dielectrics. In particular, we will develop the hypothesis that in advanced dielectric gate stacks, NBTI is composed of a "dynamic" part related to spatially and energetically close defects which can trap charge and release it spontaneously, and a "static part" at the interface or in the dielectric which cannot release charge once trapped. For this reason, the outcome of the experiments on the high-κ devices will be compared to the results of equivalent experiments on devices with "basic" SiO_2 gate dielectrics where the relative content of dynamic terms may be less significant. Finally, potential explanations for our observed effects will be discussed, and the consequences of the phenomenon will be evaluated.

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2. Chapter 2 – Negative Bias Temperature Instability

1.1 Issues for Space Electronics

Modification of semiconductor device characteristics resulting in reduction of circuit performance presents a major reliability concern for the production of space qualified electronics [1]. Degradation of circuit lifetime is a consequence of a variety of phenomena that contribute to reliability loss in space electronics. Among these phenomena are the effects of irradiation, hot carrier injection (HCI), and negative bias temperature instability (NBTI) [2, 3, 4]. A considerable amount of research has gone into the understanding and prevention of these issues and while all have progressed, some remain much more critical than others. For completeness, we will briefly describe the state of each issue.

i. Radiation effects

Radiation effects manifest themselves in several different ways. Perhaps the most critical is cumulative long term ionizing damage due to energetic protons and electrons also know as total ionizing dose (TID) [2]. TID results in V_{th} shifts, timing skews, and leakage current. Fortunately, TID is proportional to l^2 where l is the gate oxide thickness; therefore in heavily sub-micronic devices l is so small that TID becomes less relevant. Additionally, there are a series of radiation phenomena called single-event effects (SEE) [2] that are often less destructive than TID but can still be detrimental to a mission if not properly addressed. SEEs are caused by energetic particles passing through the active area of a circuit creating electron-hole pairs. This

can lead to single-event upsets such as bit-flips in a register, or single-event latchup which results in increased operating current. As space qualified technology has evolved, the issue of reliability loss due to radiation effects such as TID, and SEEs has been largely circumvented due to a global effort to build radiation hardened circuits. This effort has resulted in many "harden by process" technologies such as buried guard rings [5], and silicon on insulator (SOI) MOSFETs, as well as many "logical hardening" techniques such as the use of redundant elements, and error detection and correction (EDAC) memories [6]. In addition, given that the dose of radiation a satellite will expect to receive is completely dependent on the satellites operational orbit, a simple way to mitigate the effects of radiation is to select a low radiation orbit. However, in a lot of cases the developers do not have flexibility with regard to the operational orbit.

ii. Hot Carrier Injection

The phenomenon of HCI arises primarily when device channel lengths are scaled below 1μm without the corresponding reduction in supply voltage. The resulting increase in vertical and lateral electric field near the MOSFET drain contact can supply enough kinetic energy to the carriers in the inversion channel to overcome the potential barrier at the semiconductor/insulator interface and depassivate Si-H bonds. The issue of HCI was reduced by the introduction of lightly-doped drains (LDD) which reduced the space charge region near the drain-end of the channel thereby reducing the electric field [2]. At the same time, the evolution to lower gate voltages reduced the effects of HCI by similarly lowering the drain field.

iii. Negative Bias Temperature Instability

The physical mechanisms related to the phenomena described above are well understood and consequently the more critical issue moving forward is the more puzzling one. NBTI is a key reliability issue for advanced p-channel MOSFET technology [1,7]. As described in chapter 1, NBTI results in an increase in device threshold voltage and a consequent decrease in source-drain current and transconductance. This poses a major concern for the reliability of space qualified electronics as it can modify timing paths and increase the probability of circuit failure. At the present time, nobody truly understands the physical origin of NBTI, although some would claim they do. In the next section we will discuss a couple of the previous attempts to model the phenomenon.

2.2 Physical Mechanism behind NBTI

Efforts to explain the origin of NBTI have evolved over time from the most basic scenarios in which the phenomenon was attributed to a single mechanism, to complicated multi-mechanism processes involving diffusion of protons or molecular hydrogen, and the capture/release of holes. This progression has been complicated by challenges surrounding the appropriate way to make stress time measurements, be it continuous stress with periodic on-the-fly sampling, or stress/measure/stress techniques. In consequence, research groups have published a variety of experimental results based on completely different measurement techniques and data analysis methodologies. Comparing results from one research group to the next is difficult and often the outcomes are contradictory.

More recently it has become widely acknowledged that multiple mechanisms are responsible for the threshold voltage degradation observed in NBTI. Specifically, experimental data supports both a rapid charge trapping mechanism that can be easily recovered, and a slower but possibly permanent mechanism which is prominent in the long time domain. The origin of these mechanisms has yet to be determined; however, several research groups have put forth models to explain the phenomenon. None of the following models can accurately predict the behavior we have observed in our experiments; nevertheless, examination of the previous modeling attempts and in particular, understanding where they have failed, builds valuable knowledge and is essential for the completeness of this study.

i. The Reaction Diffusion Model

The original Reaction Diffusion (RD) [4] model for NBTI was undoubtedly the simplest case scenario. It involved only a single mechanism which resulted in the creation of an interface state, similar to those created in hot carrier injection. In this model a hole from the inversion channel, in the presence of a vertical electric field induced by the surface potential, is attracted to the semiconductor/insulator interface where it interacts with Si-H bonds created during passivation of the dangling Si bonds at the interface. This interaction was believed to weaken the Si-H bond to the point that it would break. At elevated temperature the Si-H bonds dissociate and subsequently the neutral atomic hydrogen captures a hole and becomes positively charged. The end result of this reaction,

$$Si_3 \equiv SiH + h^+ \rightarrow Si_3 \equiv Si^{\bullet} + H^+$$

is a silicon dangling bond which we call an interface state, and a positively charged hydrogen also called a proton. With the assistance of the vertical field, the proton would drift deeper into the oxide and become trapped. The RD model predicted magnitude dependence on temperature and t^{α} time dependence over all time domains.

As curiosity surrounding NBTI grew, extensive experimental results began to reveal shortcomings in RD theory. Although the model could explain the degradation of threshold voltage under constant bias stressing, it failed to address the recovery dynamics. Furthermore, the ability of a hole from the inversion layer to depassivate the Si-H bond had come into question [8]. As a result, various extensions of RD theory tried to address these issues but with minimal success. In our own experiments we have found additional evidence that RD theory is not physical. This involved showing that the time dependence of the effect does not follow the t^{α} behavior as predicted. We will discuss these results in detail in chapter 4.

Ultimately, it became clear that a single mechanism model based on the generation of interface states could not explain the time dependence or the recovery dynamics associated with NBTI. Consequently, the idea of a two component model was accepted to be more physical. The creation of interface states as described by RD theory is still believed to be one of the contributing mechanisms; however, the means by which the interface states are created remains in question. As for the second mechanism, we envision the rapid charging of defects in the oxide from holes in the inversion layer. The question remains as to how the holes overcome the potential barrier at the interface;

nevertheless, these trapped charges can apparently be rapidly filled and discharged, accounting for the recovery aspect of NBTI.

ii. Two Stage Model

A more elaborated multi-mechanism explanation is the two stage model proposed by T. Grasser, et al [9]. In this theory the precursor for the phenomenon is a neutral interfacial oxygen vacancy, which upon the capture a hole, creates a positive defect called an E'_γ center. Next, the emission of a hole (electron capture) neutralizes the defect at which point the structure can either relax back to the original oxygen vacancy precursor, or re-capture a hole and return to the E'_γ state. This is the mechanism believed to account for the rapid charging and recovery dynamics observed in NBTI. As for the second mechanism, the E'_γ center can interact with the hydrogen passivating a neighboring silicon dangling bond at the interface. Simple thermodynamic arguments [10] show that it is energetically favorable for the hydrogen to migrate to the E'_γ center leaving behind an interface state whose charge will depend on the position of the Fermi-level. An illustration of this mechanism is shown in FIG 2-1.

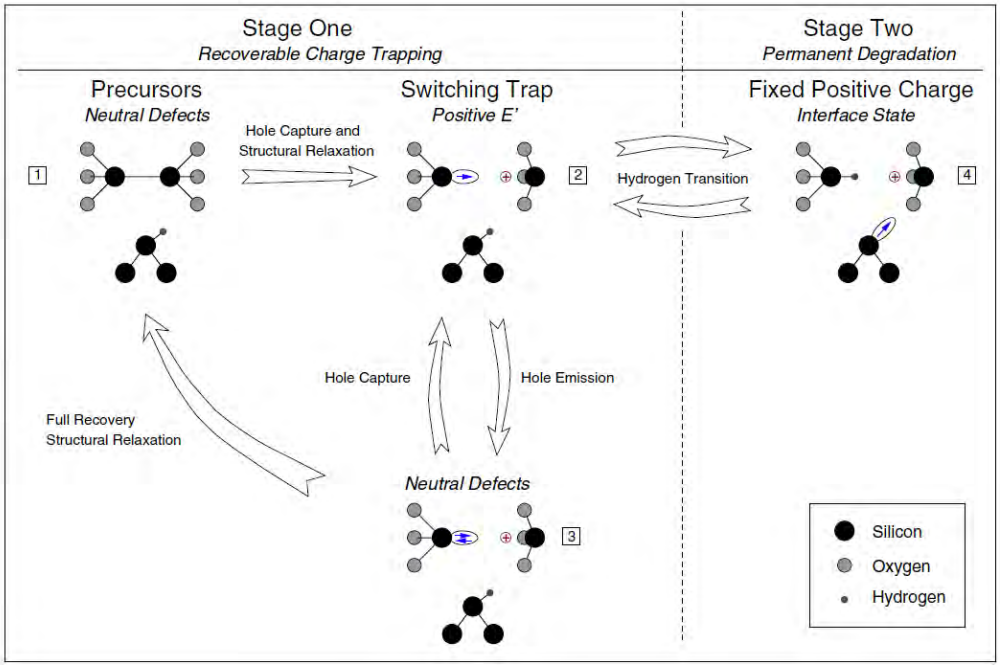

Figure 2-1) Two stage model proposed by T. Grasser et al. Stage one is based on the HDL model for switching traps. Stage two illustrates a hydrogen transitions which results in the creation of an interface state.

This model resolves issues not addressed in the previous RD model such as variable time dependence and depassivation energies of hydrogen; however, the theory is not without question. In particular, some potential concerns arise when assuming all the mechanisms associated with NBTI happen at the interface and not in the bulk of the dielectric. This concept is contradictory to experimental results showing modification of degradation characteristics dependent of the density of defects in the "bulk" of the gate dielectric [11]. Additionally, the recoverable charging mechanism in this theory is based on a mechanism proposed by the Harry-Diamond-Laboratories (HDL); however, it has been shown [8] that resultant potential barriers in that mechanism are not deep enough to sustain the positive charge and consequently the system immediately relaxes to its initial oxygen vacancy precursor state. Nevertheless, its inclusion of multiple processes is

certainly more physical than previous single process explanations, thus we believe it is a step in the right direction.

iii. Dynamic Stress Model

Some groups have elected to concentrate on the dynamic operation characteristic of CMOS circuits. A group from ASU [12] integrated dynamic voltage scaling and sleep mode into their circuit aging prediction model. Ultimately, they combined the RD theory [4] with a trapping/detrapping model [13] then developed an interface to introduce a variety of active and sleep periods. Their model attempted to predict threshold voltage degradation resulting from a combination of charging and relaxation times. They went on to examine the behavior of NBTI under a variety of different supply voltages (Vdd) arriving at the expected conclusion of increased V_{th} degradation with increased Vdd.

This model addressed some key aspects involved with development of a reliability lifetime predictor formula for realistic circuit operation. However, it is based on the physical mechanisms as predicted by the RD model in combination with a hole trapping/relaxing process in the bulk of the dielectric which is not understood. As a result, there is still an enormous amount of improvement to be made.

Examination of these models has offered some valuable insight into the possible contributing mechanisms of NBTI. Although none of them can fully explain the results we will discuss in Chapter 4, each of them conveys important concepts to consider when developing our own explanation of the phenomenon. It is important to note, however, that deciding between theoretical models is not a primary objective for this thesis. Rather, the intention of this thesis is to advance our understanding of physical mechanisms relative to

NBTI in advanced dielectrics and to unveil to relevant variables and their associated dependencies on time and gate dielectric field magnitude.

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3. Chapter 3 – Experimental Methodology

When considering the effects of time dependent trap charging as one does in NBTI measurements, there are a wide variety of experimental procedures for performing stress time measurements. From the classical start-stop methods to more modern on-the-fly techniques, it is important not only to be able to capture the **charging** mechanics, but also the charge relaxation phenomena as well. Our second experimental objective was, *study NBTI in advanced high-κ dielectrics*. Accordingly, we have performed a series of experiments on HfSiON technology to examine different features of the NBTI for the purpose of gaining a better understanding of the physical origin behind the phenomenon. This involved studying the time and magnitude dependence of threshold voltage shift on ambient temperature, the relative dependence on vertical electric field in the gate oxide (perpendicular to the inversion channel), the dependence on the electric field in the lateral sense (source-drain), and the dependence on charge density in the inversion channel. To address our third objective, *compare to the results of HfSiON experiments to equivalent experiments on devices with "basic" SiO_2 gate dielectrics*, we persisted to explore these effects on devices with SiO_2 gate dielectric stacks as well. One of the more challenging aspects of this study was acquiring samples that would be comparable. Though we never achieved this to the extent we would have preferred, we were able to acquire state-of-the-art HfSiON, and SiO_2 samples; details of their fabrication will be discussed below. In addition to experiments concerning our understanding of the physical mechanisms in NBTI, we performed other experiments that explored traditional stress/measure/stress methods primarily for the purpose of comparison to our continuous stress data. This allowed us to extract information about the potential underestimation of device reliability

lifetime depending on the chosen measurement protocol; an important piece to the puzzle for developing a reliable predictor formula. Finally, we performed rapid data acquisition measurements in a continuous mode to increase our resolution in the sub 1 second time regime. This was very important for the support of a multi-mechanism NBTI process [1] and opposed the single mechanism [2] process that was initially proposed.

3.1 Measurement Equipment

The majority of these experiments were performed at the Air Force Research Laboratories for the Space Electronics Branch. The samples under test were mounted on a temperature controlled vacuum chuck. Standard electrical MOSFET characteristics were measured using either the HP 4156 analyzer or the Keithley 4200 SCS measurement system. For our experiments, both of these systems provided a great deal of functionality with regards to manipulation of the voltages, and measurement intervals. The data acquisition time limitations of the HP meant that it was advantageous to use the Keithley when performing measurements that required high resolution in the short time. Nevertheless, the HP was more than adequate for executing the longer life tests.

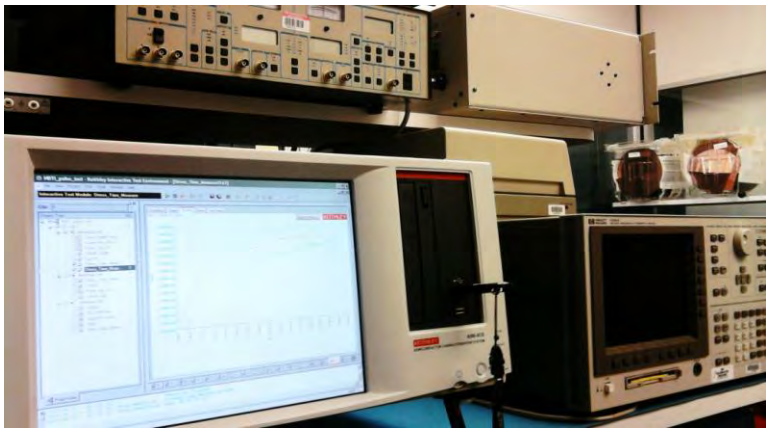

Figure 3-1) Keithley 4200 SCS measurement system and the HP 4156 semiconductor parameter analyzer

Another advantage of the Keithley was the interactive test environment (ITE) software shown open in the active window in FIG 3-1. This ITE provided a user friendly way to set up continuous stress experiments, and stress/measure/stress experiments, as well as provided a path to arrange synchronized, rapid, execution of multiple tests back to back. The most valuable feature of the Keithley 4200 system is its potential to execute a complete $I_{ds}(V_{gs})$ sweep in ~100ns! Assuming an appropriate level of accuracy is achieved during the acquisition of the curve, this method will ultimately allow for reduced approximation in determination of the full effect on threshold voltage as a result charge trapped in the gate oxide.

3.2 Device Fabrication

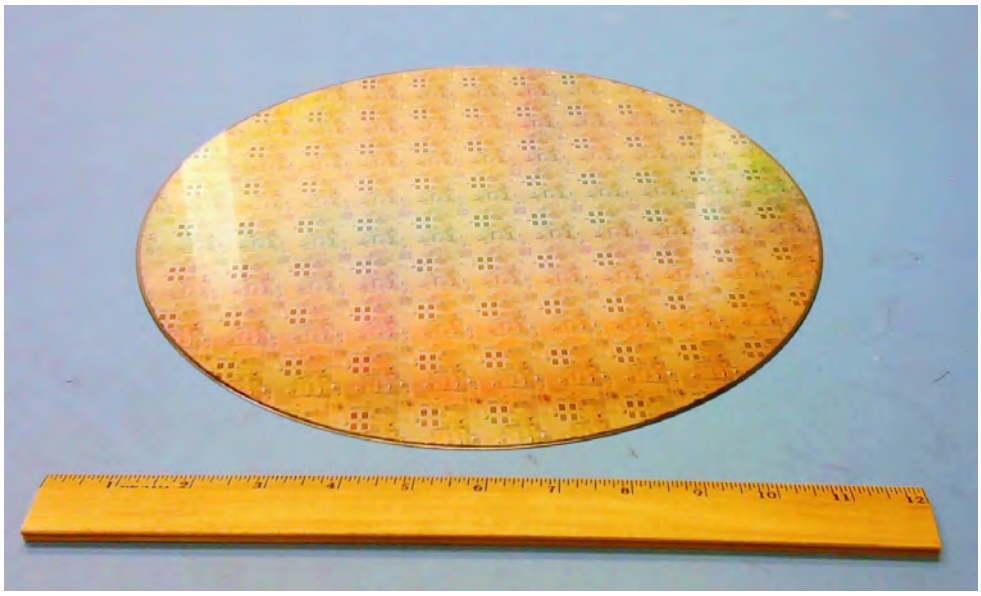

Figure 3-2) 300mm Wafer from Texas Instruments. Variety of technologies including 32nm pMOS & nMOS

Most of the experiments in this study were performed on a set of twenty-five 300mm test wafers from Texas Instruments; FIG 3-2. The entirety of the lot was built using a high-κ HfSiON gate dielectric stack optimized for 32 nm technology. However, each pair of wafers in the lot was manufactured using a slightly different processing step (for example, different LDD implant). For the purpose of obtaining comparable results then, all of our measurements were performed on a single wafer. Because the original purpose of the lot was to evaluate gate stack performance and reliability for a variety of technology nodes, there was a wide range of device channel lengths available ranging from 10μm to 32nm. The devices used in the experiments reported here were primarily p-channel MOSFETs with 1 μm channel lengths. This length minimized the potential for short channel effects. Additionally, some devices with 10, 0.7, or 0.3 μm channel lengths were also used. The gate dielectric stacks were formed [3] of chemically oxidized Si (approximately 1 nm of SiO_2) upon which HfSiO was deposited using the technique of atomic layer deposition (ALD). The hafnium and silicon precursors in the ALD process were $Hf[N(CH_3)C_2H_5]_4$ and $Si[N(CH_3)C_2H_5]_4$ respectively. The stack was then nitrided using the process of post deposition annealing in NH_3. The metal electrodes were formed of physical vapor deposited (PVD) TaN. A conventional CMOS flow completed the fabrications process. FIG 3-3 is a magnification of the CMOS array showing the contact pads and, because there is only one metal layer, the physical features of the individual transistors.

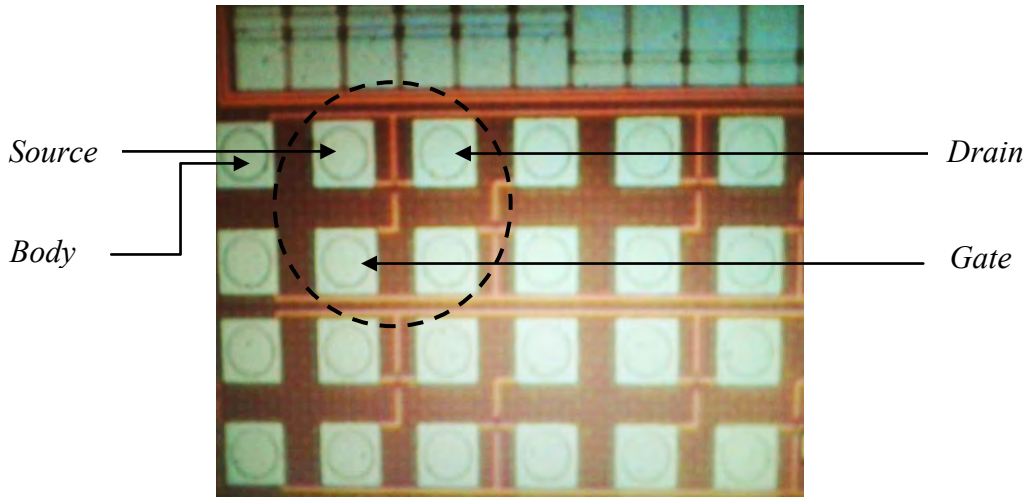

Figure 3-3) Probe contacts for CMOS array on 300mm TI wafer. Specifically labeling the contacts of a 45nm p-channel MOSFET

Given that NBTI is strongly dependent on the physical properties of the gate oxide, we performed additional experiments on two sets of devices with the "classical" SiO_2 insulator. These dielectrics were much less complex than those of the high-κ devices simplifying the possible physical explanations, thus providing a great "baseline" for our physical interpretation of the data. The first set of devices were fully depleted, silicon-on-insulator (SOI) p-channel MOSFETs from Lincoln Labs at MIT. They contained a 2.6nm SiO_2 gate oxide and their channel lengths ranged from 130nm to 8μm. The second set was from IBM‟s 130nm process. Details of their manufacture are available at ibm.com under IBM‟s industry standard 130nm CMOS technology family. The relevant parameters in this context are the thickness and composition of the gate oxide which for these devices was 3.3nm and SiO_2 respectively.

3.3 Measurement Methods

NBTI has been recognized as a reliability issue since the mid-1960"s [4]. The first NBTI experiments were performed using a stress/measure/stress technique which we call a "start-stop" measurement. Devices under test would first be heated to between 100 °C and 200 °C and an initial $I_{ds}(V_{gs})$ sweep would be performed. After a finite amount of time in which a stressing voltage was applied to the gate electrode, the stress would be temporarily removed and another $I_{ds}(V_{gs})$ curve would be acquired. Immediately following the acquisition of the data, the stressing voltage would be re-applied to the gate and the process would repeat. This method suffers from the fact that during the time it takes to stop the bias stress and perform the $I_{ds}(V_{gs})$ sweep (a few seconds), information is lost due to the relaxation of trapped charge in the oxide [5], particularly at the Si-SiON/HfSiON interfaces. Taking this data to be exact would result in both incorrect physical models, and inaccurate lifetime reliability predictor formulas. For the purpose of completeness we have used the start-stop method and subsequently compared the results to the more modern measurement methods. The details of these measurements vary between experiments and will be discussed below.

Researchers realized that until there is a way to acquire an IV curve in times less than the shortest relaxation time of trapped charge, we cannot get an accurate representation of the full magnitude of NBTI from traditional start-stop measurements. New, but approximate, methods for extracting a device"s threshold voltage without having to interrupt the device"s stressing conditions have been developed; typically they are referred to as "on-the-fly" measurements. For example, continuously measuring the frequency degradation of a ring oscillator and assuming that it is proportional to change

in threshold voltage is an on-the-fly method used to measure the reliability of a device under realistic circuit operation [6]. In our experiments we are more interested in the physics of the phenomenon so we have adopted a continuous stress implementation that allows us to see the maximum effect of NBTI on a single p-channel MOSFET. The details of this method will be discussed below. Using this continuous technique the assumption is made that any traps charged through application of the stress will remain charged throughout the entire $I_{ds}(t)$ measurement and this will then reflect the full magnitude of the total charged trapped during the stressing period.

For the temperature dependence experiment we employed two measurement techniques. Using the start-stop technique, I_{ds} measurements were made as a function of the applied gate-source potential V_{gs} swept from 0V to -1.5V with the source-drain potential maintained at -0.9V. Source and substrate were grounded. In between $I_{ds}(V_{gs})$ acquisitions, the gate and drain electrodes were subjected to a bias stress of V_{gs} = -1.5V and V_{ds} = -0.9V respectively. Bias stress time intervals varied from 10 s to 300 s and accumulated to 3600 s. At each time point, the total time required to remove the gate voltage and perform the $I_{ds}(V_{gs})$ sweep was measured to be between 3.5 and 5 s. Alternatively, in a continuous technique, the source-drain current was probed every 5 seconds without the requirement to turn off the bias. This data was accumulated at three temperatures; 95 °C, 125 °C and 155 °C.

In the next set of experiments we explored the time and magnitude dependence of NBTI on both vertical and lateral electric fields. As in the previous case, we used two measurement techniques for each set of data. To specifically analyze the vertical electric field dependence with a start-stop technique, $I_{ds}(V_{gs})$ measurements were made with V_{gs}

swept from 0V to -2.0V, while V_{ds} was maintained at -2.0V. In between data acquisitions, the devices were subjected to a bias stress at one of four gate voltages; -2.0V, -1.7V, -1.5V and -1.3V. Since this placed the devices in the inversion mode, the approximate potentials across the dielectric stack were –1.1,-0.8,-0.7 and –0.5 V in the region of the source contact. The uniformity of the vertical field along the channel will be discussed later. Furthermore, in the simplest approximation of a two layer SiON(1 nm)/HfSiON (2 nm) structure, the potential would be non-uniformly divided resulting in a significant field in the SiON layer and a much smaller field in the high-k HfSiON part [5]. In these experiments, the bias time intervals varied from 10s to 120s and were accumulated to 2290 s total. V_{ds} was maintained at -2.0V during the bias stressing intervals and in all cases a constant temperature was maintained at 175C. For the second approach, the devices were biased in the saturation regime at each of the four gate voltages described above. As mentioned previously the transition from $\Delta I_{ds}(t)$ to $\Delta V_{th}(t)$ is approximate but justified.

We developed two unique methods for examining the current density and lateral electric field dependence. In both methods we employed the continuous measurement technique. In the first approach, we increased the device channel length by an order of magnitude while maintaining the same channel width, oxide thickness, and stressing voltages. The effect of this was to decrease the source-drain current by an order of magnitude and proportionally decrease the magnitude of the electric field in the lateral direction. In a second approach, we were particularly interested in the fast trap charging effect as the devices made the transition from saturation to linear regime. This transition was achieved by reducing the source-drain voltage. To adequately capture this data it was

necessary to increase the resolution in the early time. As a result, these measurements were performed using the Keithley 4200 SCS system in a continuous mode wherein I_{ds} was probed approximately every 0.75 seconds without the interrupting the stress. The devices were all stressed at a temperature of 175C, V_{gs} = -2.0V, and V_{ds} took the values -2.0V, -1.7, -1.5V, -1.25V, -1.0V, -0.75V, -0.5V, -0.25V, and -0.1V. We used 9 different source-drain voltages to give us more resolution as the device operation varied from the saturation region into the linear regime [7]. The results of these tests were without a doubt the most surprising/intriguing of the entire study and will be discussed in detail in Chapters 4 & 5.

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4. Chapter 4 – Experimental Results

We performed a variety of experiments on p-channel MOSFETs with HfSiON gate dielectric, and compared the results to those on SiO_2 devices. These experiments were developed to test time and magnitude dependencies of threshold voltage shifts under an assortment of different stressing conditions. The goal was to decouple the electric field, temperature, and charge density components that are responsible for NBTI in order to improve our understanding of the physical mechanisms involved. Before we present the experimental results, it is necessary to describe our methodology for translating continuous current measurements into threshold voltage shifts. In the subsequent section we will justify our data interpretation methods, and discuss the approximations involved.

4.1 Data Analysis Methodology

In order to appropriately analyze the data we must first translate change in source-drain current with time $\Delta I_{ds}(t)$ to change in threshold voltage with time $\Delta V_{th}(t)$. This is simple for the case of the discrete stop-start method because we have a complete $I_{ds}(V_{gs})$ data set. By plotting the square root of the I_{ds} in the saturation regime [1],

$$I_{ds}^{1/2} = [\ (W/2L)\ C_{ox}\ \mu\ ]^{1/2}\ [V_{gs} - V_{th}^{o}\ ], \qquad (4\text{-}1)$$

as a function of V_{gs} then taking the derivative, we obtain the slope of the "post threshold" region. Using slope intercept formula we can calculate V_{gs} for $I_{ds} = 0$ which, from EQ 4-1, is equal to the threshold voltage.

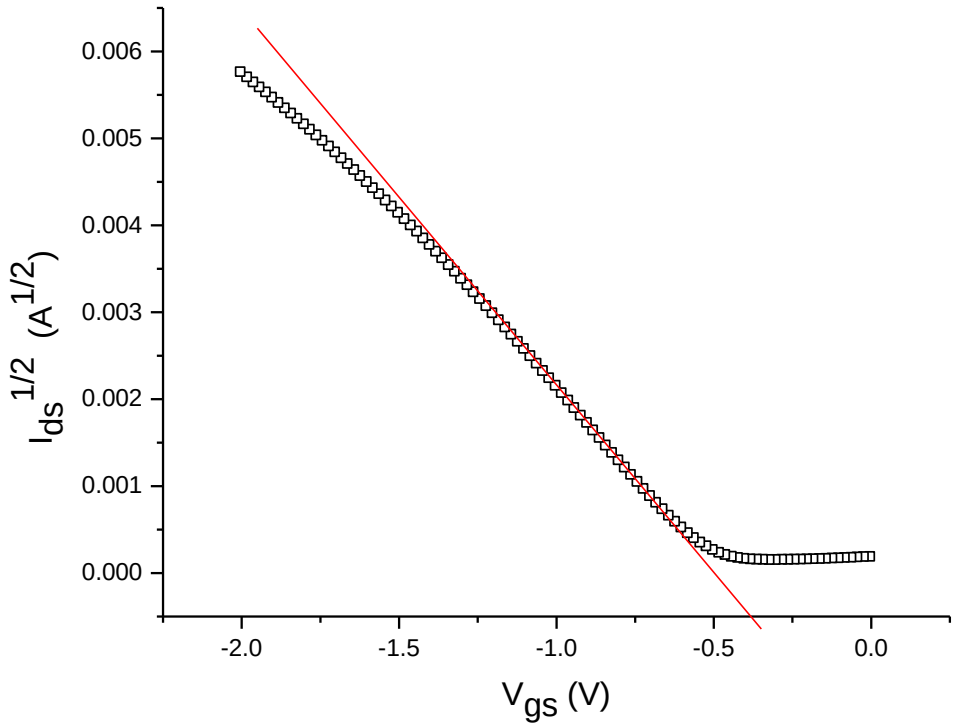


Figure 4-1) Square Root of I_{ds} as a function of V_{gs}. The straight line is a guide to the eye

Translation of $\Delta I_{ds}(t)$ into $\Delta V_{th}(t)$ for the continuous method, where a single unique point on the $I_{ds}(V_{gs})$ curve is captured at equal points in time, is considerably more complex than the equivalent analysis on the start-stop data set since it involves approximations. EQ 4-1 contains two parameters which can vary due to charge trapping/interface state generation, inversion channel carrier mobility μ, and V_{th}. In order to eliminate one of these variables we examine first the situation for μ. There are at least two reasons why the carrier mobility can change. First we consider the effect of vertical field resulting from V_{gs} [2]. Electric field dependent mobility is evidenced by FIG 4-1 where we have plotted $(I_{ds})^{1/2}$ as a function of V_{gs}. From EQ 4-1, a plot of $(I_{ds})^{1/2}$ versus

V_{gs} should be a straight line of slope $[(W/2L)\, C_{ox}\, \mu]^{1/2}$ and should intercept the V_{gs} axis at V_{th}. Disregarding the sub threshold behavior, the curvature at large V_{gs} is a result of electric field dependent mobility and can be expressed as [2]:

$$\mu = \mu_o/(1 + \varphi\, [V_{gs} - V_{th}^{o} - \Delta V_{th}]) \tag{4-2}$$

where φ is a constant and V_{th}^{o} is the threshold voltage at t=0 before the device has been subject to stressing. From EQ 4-2 it is clear that assuming the carrier mobility to be a constant in the data interpretation methodology has the potential to introduce an error depending on the magnitude of the change in V_{th} and the value of φ. In the case of our continuous measurements, we maintain a unique set of V_{gs} and V_{ds} values, and variations in V_{th} are small with respect to V_{th}^{o}. As for the constant φ, this can be deduced by fitting $I_{ds}^{1/2}(V_{gs})$ with the full formula in EQ 4-1, including the modification of mobility term in EQ 4-2. In doing this, we determined φ to be on the order of 10^{-1}. As a result, to a first approximation it is reasonable to conclude that we can neglect electric field dependent mobility as expressed in EQ 4-2. The next step is to determine how trapped charge can modify the carrier mobility. We assume that trapped charge in the oxide, regardless of position (close to the Si/SiO_2 interface or in the bulk of the dielectric), can be represented by the quantity ΔN_t. The resulting threshold voltage shift from the trapped charge can then be expressed as [3]:

$$\Delta V_{th} = -\Delta N_t\, q/C_{ox} \tag{4-3}$$

where q is the elemental charge. Given that this term modifies the threshold voltage, it changes the electric field in the vertical direction as well. The change in electron mobility as a result of trapped charge can be written as [4]:

$$\mu = \mu_o/(1 + \alpha'\Delta N_t) \tag{4-4}$$

where α' is a constant. Rearranging EQ 4-3 and substituting into EQ 4-4 yields:

$$\mu = \mu_o/(1 - \alpha' \Delta V_{th} C_{ox}/ q) \tag{4–5}$$

Substituting EQ 4-5 into the general square law formula expressed in EQ 1-1 we arrive at the expression:

$$I_{ds} = [W/2L]\, C_{ox}\, [\mu_o/(1 - \alpha' \Delta V_{th}\, C_{ox} / q)]\, [\{V_{gs} – (V_{th}^{o} + \Delta V_{th})\} V_{ds} – 1/2V_{ds}^{2}] \tag{4-6}$$

This expression now contains a parameter that accounts for the modification of mobility as a result of trapped charge, and a parameter that influences the device threshold voltage. EQ 4-6 can be further simplified by removing the dependency of ΔV_{th} from the denominator. Starting with EQ 4-5 in the form: $\mu/\mu_o = (1 - \Delta\mu/\mu_o) = (1 + \alpha'\Delta N_t)^{-1}$. We can assume $\alpha'\Delta N_t < 1$, then by taking the series expansion we can approximate $\Delta\mu/\mu_o$ by:

$$\Delta\mu/\mu_o \sim \alpha'\Delta N_t \tag{4-7a}$$

by rearranging EQs 4-3 and 4-7a we arrive at an expression whereby the parameter α' can be determined from the slope of a ΔV_{th} versus $\Delta\mu/\mu_o$ plot:

$$\Delta V_{th} = -(q/\alpha' C_{ox})\Delta\mu/\mu_o \tag{4-7b}$$

It has been experimentally shown that α' is on the order of 10^{-13} over a wide range of temperatures [5]; additionally, threshold voltage shifts relative to NBTI are typically in the range of 10"s of mV. As a result, to a first approximation we can say that $\alpha' \Delta V_{th} C_{ox} / q << 1$ thus we can neglect charge induced mobility in EQ 4-6. The inclusion of this approximation yields:

$$I_{ds} = [W/2L]\, C_{ox}\, \mu_o\, [\{V_{gs} - (V_{th}^{\ o} + \Delta V_{th})\} V_{ds} - 1/2 V_{ds}^{\ 2}] \tag{4-8}$$

This simplified equation can be used to calculate the source-drain current after a threshold voltage shift. In addition, we know that the initial source-drain current ($I_{ds}^{\ o}$), before accounting for any changes in characteristics, can be expressed by EQ 1-1. It is then trivial to show that by taking the ratio $I_{ds}(t)/ I_{ds}^{\ o}$, we can obtain the expression:

$$I_{ds}/ I_{ds}^{\ o} = (V_{gs} - V_{th}^{\ o} - \Delta V_{th} - 1/2 V_{ds}) / (V_{gs} - V_{th}^{\ o} - 1/2 V_{ds}) \tag{4-9}$$

re-arranging:

$$\Delta V_{th} = [V_{gs} - V_{th}^{\ o} - 1/2 V_{ds}](1 - I_{ds}/I_{ds}^{\ o}) \tag{4-10}$$

This expression holds for the case that $|V_{ds}| < | V_{gs} - V_{th} |$ corresponding the linear region of transistor operation [6]. For the case of the saturation regime ($|V_{ds}| \geq | V_{gs} - V_{th} |$), we simply replace V_{ds} with $(V_{gs} - V_{th})$ [6]. Note that this could also be accomplished by starting from the saturation current law, normalizing, and then solving the quadratic which yields:

$$\Delta V_{th} = -(V_{gs} - V_{th}^{o}) \pm [2(V_{gs} - V_{th}^{o})^2 - 4(V_{gs} - V_{th}^{o})^2 (1 - I_{ds}/ I_{ds}^{o})]^{1/2}/2 \quad (4\text{-}11)$$

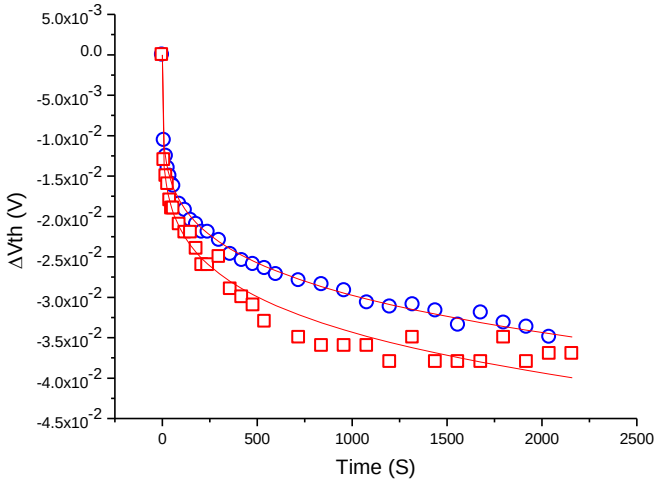
Both equations, 4-10 and 4-11, are equivalent as they relate to the analysis of a device that has been stressed in the saturation regime; however, EQ 4-11 is not valid for the linear region.

The final obstacle to overcome with this interpretation methodology was acquiring an accurate value for I_{ds}^{o}. This challenge was a result of the characterization equipment whereby the stressing voltage was applied to the gate for 1 – 2 seconds before we recorded our first data point. Because this method uses a normalization technique, it hinges on an accurate initial value. To accomplish this we extrapolate the initial linear part of the $I_{ds}(t)$ back to the origin and take that value to be I_{ds}^{o}.

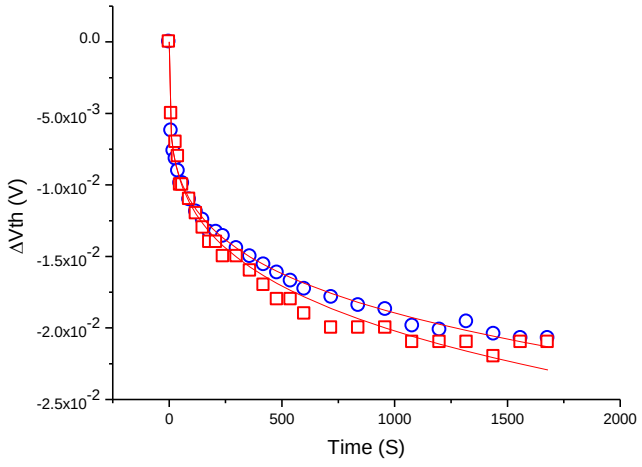
4.2 Full Curve Fit Vs Single Point Approximation

In the previous section we examined/justified the approximations required to translate $\Delta I_{ds}(t)$ in to $\Delta V_{th}(t)$ from the single point continuous stress method. We now take a look at experimental data from the HfSiON technology to gain a feeling for the amount of

error induced by these approximations. The approach for this experiment was to extract a threshold voltage shift from a complete start-stop data set with two techniques: 1) using the complete $I_{ds}(V_{gs})$ characteristic curve and extracting the threshold voltage using standard methods discussed above. 2) Using a unique I_{ds} value obtained from a complete $I_{ds}(V_{gs})$ plot at the point $V_{gs} = V_{bias}$, $V_{ds} = -2V$, then applying EQ 4-10. The result of this is $\Delta V_{th}(t)$ plots from the same data set; the first case being the most accurate. FIG 4-2 shows the result of this analysis at 4 different gate voltages and a temperature of 175C.



(a)



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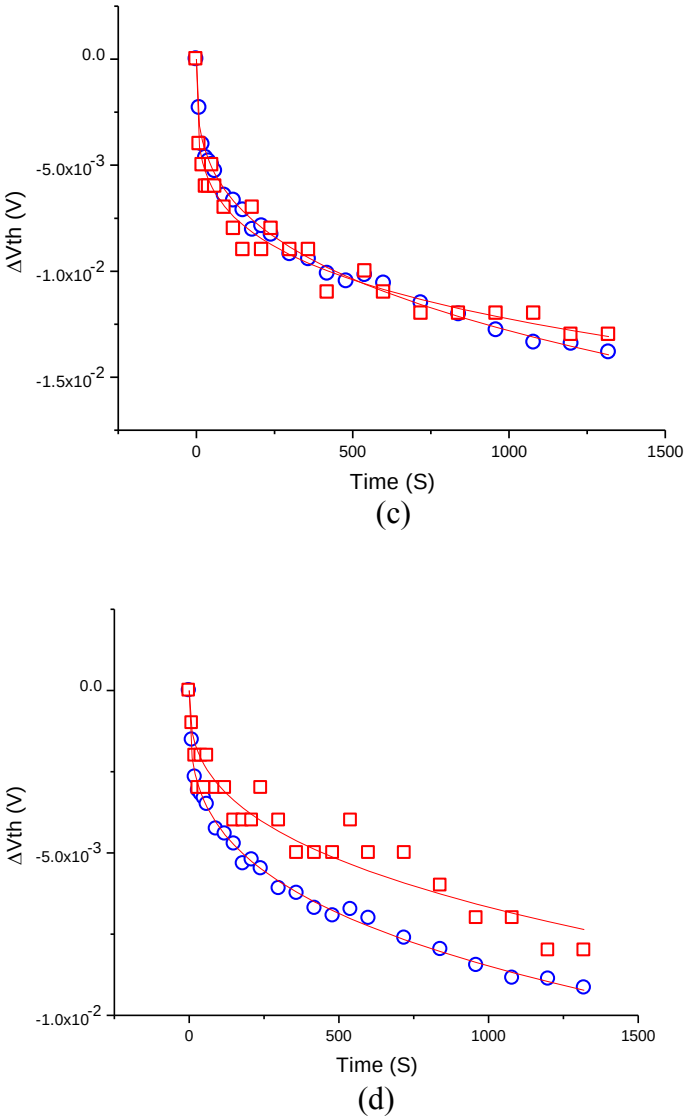


Figure 4-2) Example of $V_{th}(t)$ extracted from the start-stop method using two techniques; taking one unique point on the curve, $I_{ds}(V_{bias})$, then applying EQ 4-10 (O), using the complete characteristic curve then applying standard methods (□). Results are shown for V_{bis} of a)-2.0V, b) -1.7V, c) V-1.5V, and d)-1.3V . T=175C in all cases. Solid lines represent non-linear curve fit using $\Delta V_{th} = At^{\alpha}$.

Most importantly, this experiment confirmed that our approximations from EQ 4-10 are reasonably accurate within experimental error over a wide range of gate voltages. This was determined by fitting the data to a simple At^{α} power law then comparing the fit parameters A and α. The solid lines in FIG 4-2 are the result of the power law fit.

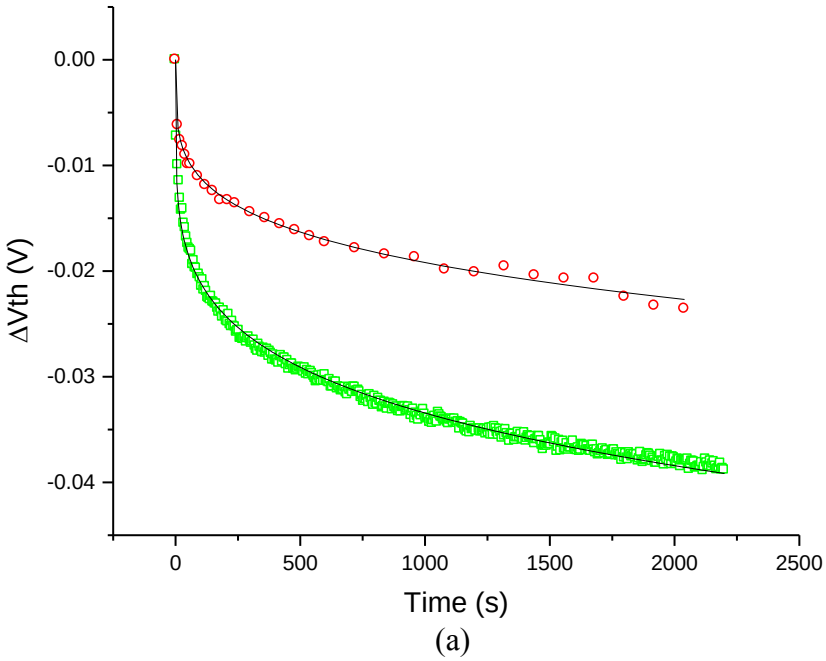
Clearly, the quality of this fit is affected by the value of V_{gs} and in general this analysis technique is very approximate. In the subsequent section we will show that assuming $\Delta V_{th}=At^{\alpha}$ is not accurate for all time domain. In TABLE 4-1 we summarize the A and α fit parameters for the approximate and exact determination of V_{th}. We conclude that our margin of error is < 5% for the stressing conditions of interest. Further analysis of FIG 4-2 raises some interesting questions; in particular, it is not yet clear whether the observed systematic variation between the two methods is a result of the approximations, or a consequence of the physical mechanisms involved. It is clear that our approximation results in a slight underestimation of the threshold voltage shift at large values of V_{gs} and a slight overestimation of the effect at small values V_{gs}. Consequently, even in the case of our continuous method, which was intended to capture the maximum effect, we still would underestimate the device reliability lifetime. It is because of this that the demand for rapid data acquisition systems has arisen. With these systems we could potentially eliminate approximations involved in our data interpretation methodology.

V_{gs} (V)	$A_{start\text{-}stop\ APPROX}$	$\alpha_{start\text{-}stop\ APPROX}$	$A_{start\text{-}stop\ FIT}$	$\alpha_{start\text{-}stop\ FIT}$
-2.0	-0.0071	.21	-0.0088	.20
-1.7	-0.0038	.23	-0.0036	.24
-1.5	-0.0026	.24	-0.0034	.24
-1.3	-0.0010	.31	-0.0006	.36

Table 4-1) α values deduced from $\Delta V_{th}=At^{\alpha}$ fits. Two methods were invoked; the start-stop method with translation into V_{th} minding approximations using EQ 4-10, and the start-stop method with exact determination of V_{th} from the full $I_{ds}(V_{gs})$ curve.

4.3 The Start-stop Method Vs The Continuous Method

The traditional measurement techniques did not take into account parametric changes that are more rapid than we can measure. In our experiments, we invoked both start-stop, and continuous measurement methods to better visualize the shortcomings of the traditional techniques. In FIG 4-3 we show a typical result of these experiments. In this particular case, two HfSiON 1μm p-channel MOSFETs were subjected to the following stress conditions: V_{gs}=-2.0V, V_{ds}=-1.7V, and T=175C. Here the start-stop curve (red circles), and continuous stress curve (green squares), are represented on a plot of threshold voltage change as a function of time ($\Delta V_{th}(t)$). As expected, analysis of the $\Delta V_{th}(t)$ curves reveals a dramatic difference in the magnitude of the measured effect dependent upon the measurement method. This is a consequence of charge relaxation during the 3-5 seconds it takes to acquire the $I_{ds}(V_{gs})$ characteristics in the start-stop experiment. The continuous technique avoids this issue by virtue of the continuous stressing voltage on the gate. In both cases, the data appears to be well fit by a simple power law which was a typical means for interpreting these NBTI degradation curves [7]. The solid black lines in FIG 4-3 are the At^{α} fits to the data.



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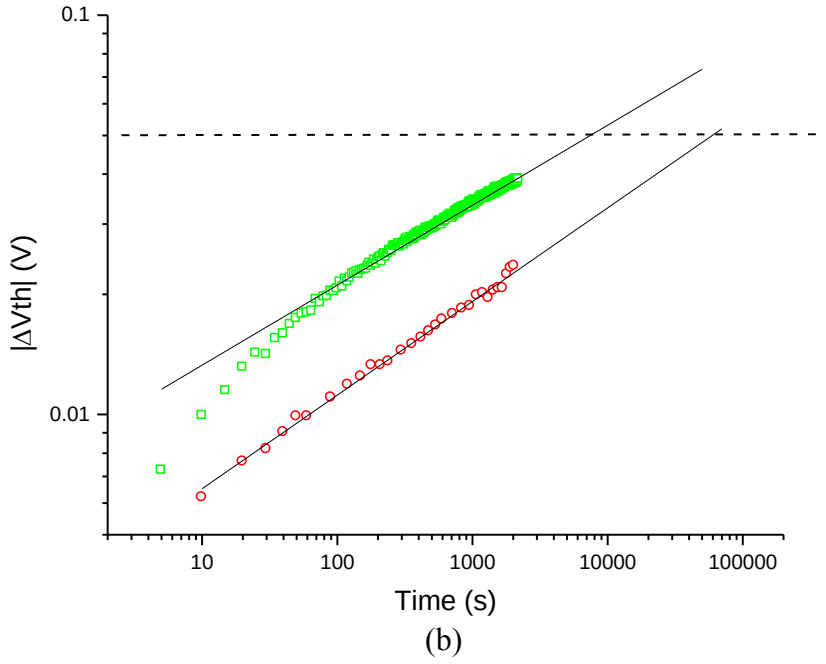


(b)

Figure 4-3) a) Comparison of $\Delta V_{th}(t)$ for the Continuous Stress Method (□) and the Start-Stop Method (O). These measurements were performed on devices stressed at -1.7V on the gate and at a Temperature of 175C. b) At^{α} fit to continuous (□) and start-stop (O), $\Delta V_{th}(t)$ measurements extrapolated out to $\Delta V_{th}/V_{th}^{o} = 0.1$ (dotted line)

Most of the early modeling attempts, primarily the Reaction Diffusion Model [8], predicted that NBTI induced threshold voltage shifts follow an At^{α} time dependence. This aspect of RD theory continues to be widely accepted among the NBTI community because it explains most "traditional" stress/measure/stress data. However, the results of our continuous stress measurements have made it clear that At^{α} fails to explain the behavior in the early time domain. FIG 4-3b reveals that sub 100s, the continuous curve (green squares) exhibits a clear deviation from the power law. Note that this is accentuated in a log plot but could easily be overlooked on a linear plot. In summary, while a simple power law fit is useful for comparing the behavior of devices at long times, it does not accurately represent the true physical mechanisms involved, certainly at short time. As a result, we have begun to explore the possibility of an initial „fast" mechanism that is overtaken by a slower mechanism at long times. This effect was not previously observed because it was masked by the inadequacies of typical $\Delta V_{th}(t)$ measurements. In Chapter 5 we will discuss this theory in more detail.

FIG 4-3b is of particular interest in relation to building a reliable lifetime predictor formula because it reveals the importance of choosing an accurate data interpretation/collection methodology. The dotted line in this figure is at $|\Delta V_{th}/V_{th}^{o}| = 0.1$ corresponding lifetime definition of 10% variation in threshold voltage. Extrapolation of the power law fits out to $|\Delta V_{th}/V_{th}^{o}| = 0.1$ exposes the magnitude of error that can be achieved as a result of the measurement technique adopted. In this particular example, the continuous curve reaches 10% loss in V_{th} at ~7500s. Conversely, it takes the start-stop curve ~58500s to reach the same level! This corresponds to 2 and 16 hours respectively or a factor of 8 difference between the two methods. The mean time to failure in these

experiments may sound surprising at first but it is important to remember that we have accelerated the physical mechanisms by application of a large vertical field and high operation temperature. There is however, no reason to believe that these results would not scale to realistic operating conditions thus it is imperative to understand the characteristics of the measurements before making any predictions about the lifetime of a circuit.

4.4 Temperature Dependence

Understanding the time and magnitude dependence of ΔV_{th} on temperature is critical when developing a model of the physical mechanisms in NBTI. Over the course of this study, we performed a large number of temperature dependence experiments on a variety of different technologies. As expected, the magnitude of threshold voltage degradation in the HfSiON technologies was significantly greater than that of the simple SiO_2 devices. This is generally accepted to be the result of a higher defect density in the high-κ dielectric. An additional observation is the fact that each technology we tested had its own unique time dependence on temperature. It is clearly evident that the mechanisms involved in NBTI are strongly dependent on the gate dielectric processing steps making a generic reliability lifetime formula very complicated.

In FIG 4-4 we show the results from one of our first temperature dependence experiments. In this experiment we performed on-the-fly (OTF) continuous stress measurements at three temperatures; 95C, 125C, and 155C, while maintaining V_{gs} and V_{ds} at -1.5V and -0.9V respectively. Bearing in mind the limitations discussed previously, we subsequently fitted the data to the simple $\Delta V_{th}=At^{\alpha}$ power law from which we were

able to deduce α(95C)=0.182, α(125C)=0.189, and α(155C)=0.187. Clearly we observed magnitude dependence in the direction of increasing degradation with increasing temperature. However, there did not appear to be a time dependence on temperature associated with this effect.

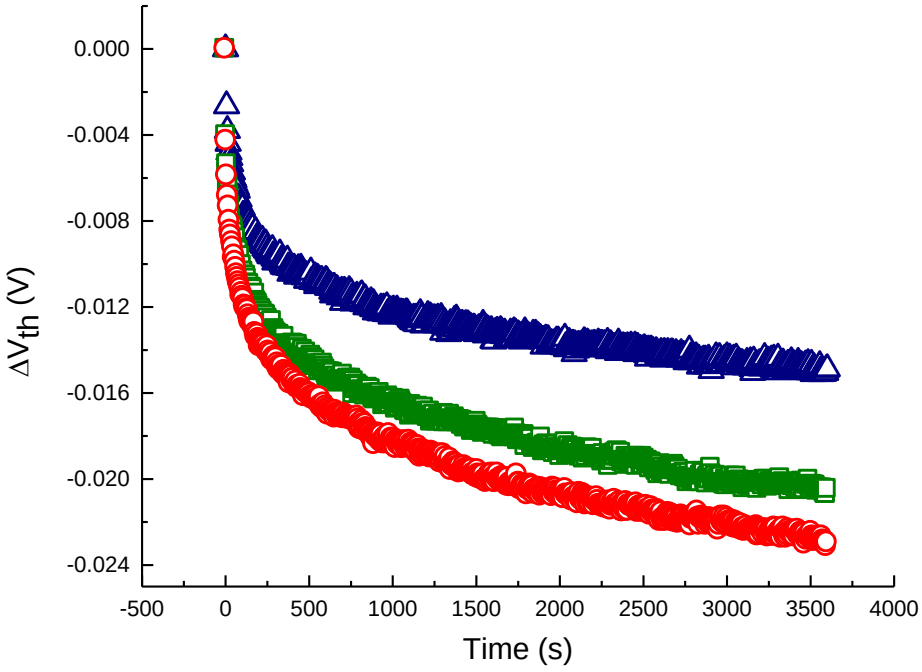


Figure 4-4) Threshold voltage shifts resulting from NBTI as determined from continuous bias method for T=95C (Δ), T=125C (□), T=155C (O). Gate dielectric stack was high-κ HfSiON

The curves represented in Fig 4-4 have been fitted to an At^{α} power law. Above we deduced the α fitting parameter at each stressing condition which revealed no time dependence on temperature in the HfSiON samples. Secondly, we examined the prefactor

A. This prefactor contains a temperature activated term which is assumed by the RD model to be [8]:

$$\Delta V_{th} = A_o e^{-E_A/kT} t^{\alpha} \tag{4-12}$$

thus A $\propto A_o e^{-E_A/kT}$. Consequently, a plot of the natural logarithm of the experimentally determined prefactor as a function of $1/T$ will yield the activation energy of the mechanism. In FIG 4-5 we show $\ln(A_o e^{-E_A/kT})$ vs $1/T$. Linear fitting yields E_A=0.085±0.012 eV.

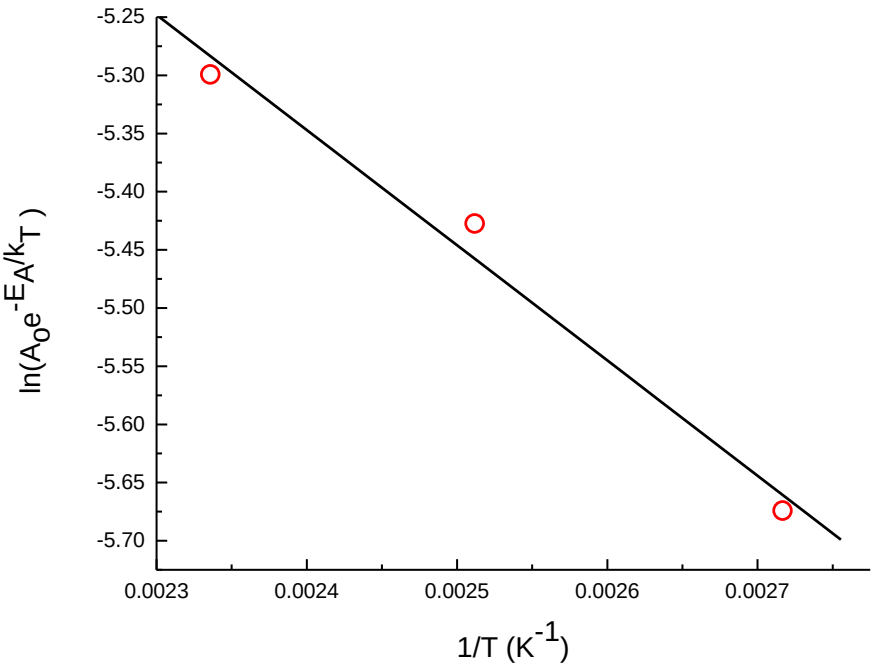


Figure 4-5) $\ln(A_o e^{-E_A/kT})$ vs $1/T$ plotted using the prefactor fitting parameter from the data shown in FIG 4-4

Given that we have deduced the activation energy of the mechanism as well as the time dependence, it is now possible to determine the "real" lifetimes at normal operation

temperatures. To do this we again use a lifetime definition of 10% variation in $V_{th.}$ Extrapolating the power law fits to the data at 155C out to $|\Delta V_{th}/V_{th}|$~0.1, we conclude that the device V_{th} will vary by 10% in 3.43 days **under accelerated conditions**. Because we have determined the activation energy, we can take the ratio of the exponentials in EQ 4-12 and deduce a multiplying factor for the reliability lifetime at normal operating temperatures. Accordingly, we determined at 80 C, normal operation temperature, the HfSiON devices V_{th} will shift by 10% in 68.6 days. Note that this is the life time under normal operation temperatures; however, it is still accelerated by the magnitude of the gate voltage and the fact that we maintain the stress continuously throughout the experiment. Under normal circuit operation, one would expect a finite amount of "down time" in which the trapped charge would relax thus lengthening the lifetime. Taking into account factors such as this, make the development of a generic lifetime predictor formula very complex.

4.5 Dependence on the Vertical and Lateral Electric Fields

It is well know that the vertical electric field is responsible for triggering the degradation mechanisms involved in NBTI. In our experiments we explored the time and magnitude dependencies on the vertical electric field across the oxide, and lateral electric field across the carrier channel. In the first instance we examined the effect of vertical field on our HfSiON samples. In these experiments devices were stressed at one of the following unique gate voltages; -2.0V, -1.7V, -1.5V and -1.3V. The temperature was maintained at 175C and V_{ds}=-2.0V. As in the previous experiments, continuous current measurements were performed using the technique described in Chapter 3, then

subsequently translated into threshold voltage shifts via EQ 4-11. The $\Delta V_{th}(t)$ curves in FIG 4-6 were measured on 1μm channel devices. We observed threshold voltage shifts of the order of 10mV at 1000s for devices stressed with -1.3V on the gate (circles). Comparatively, devices stressed with -2.0V on the gate (triangles) exhibited threshold voltage shifts of the order of 50mV at 1000s. We believe the resulting 5x increase in device degradation from -1.3V to -2.0V is a consequence of the stronger vertical electric field accelerating the charge creation/trapping mechanisms associated with NBTI. In chapter 5 we will discuss trap charging kinetics.

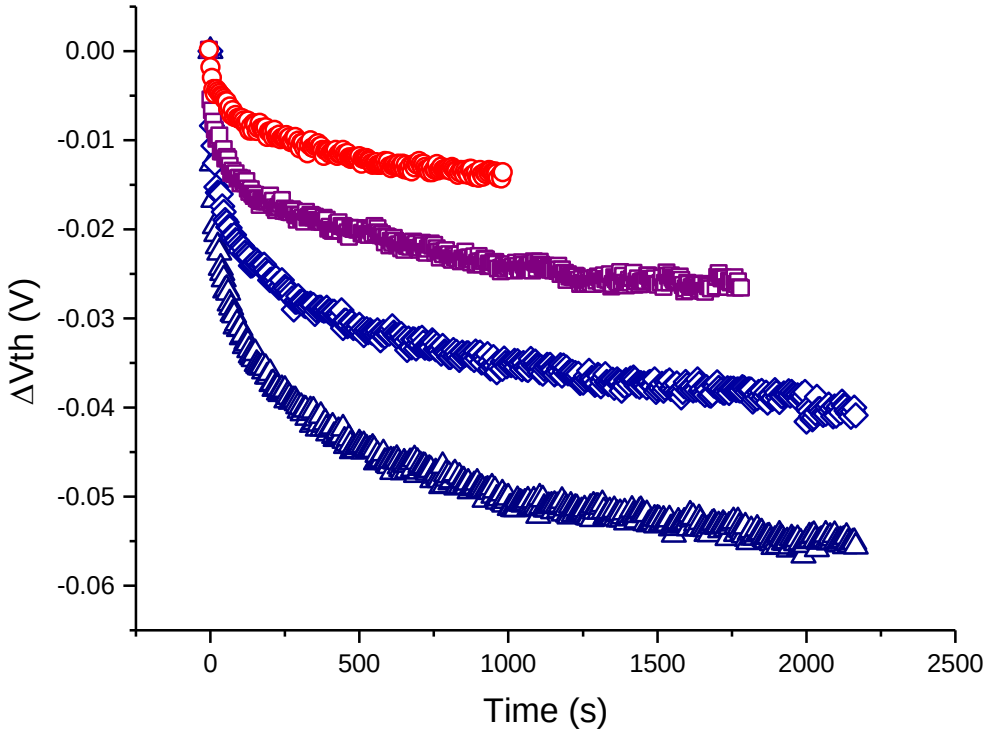
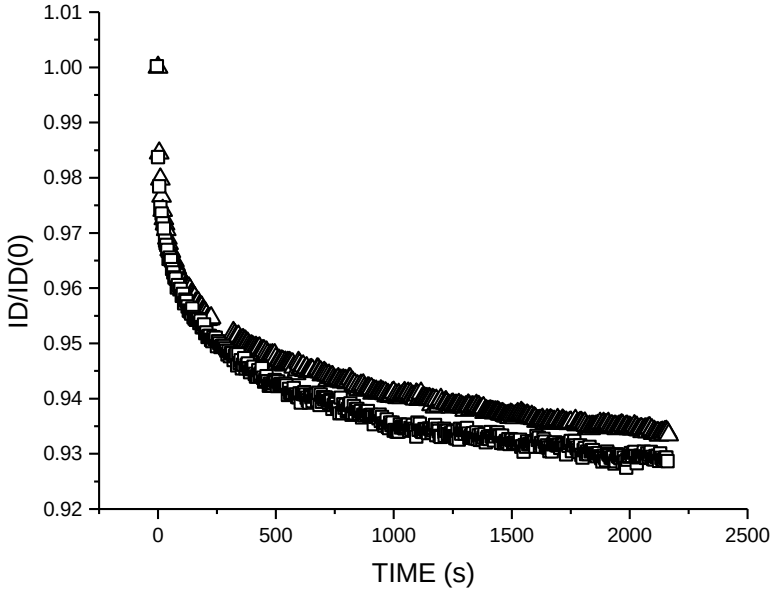
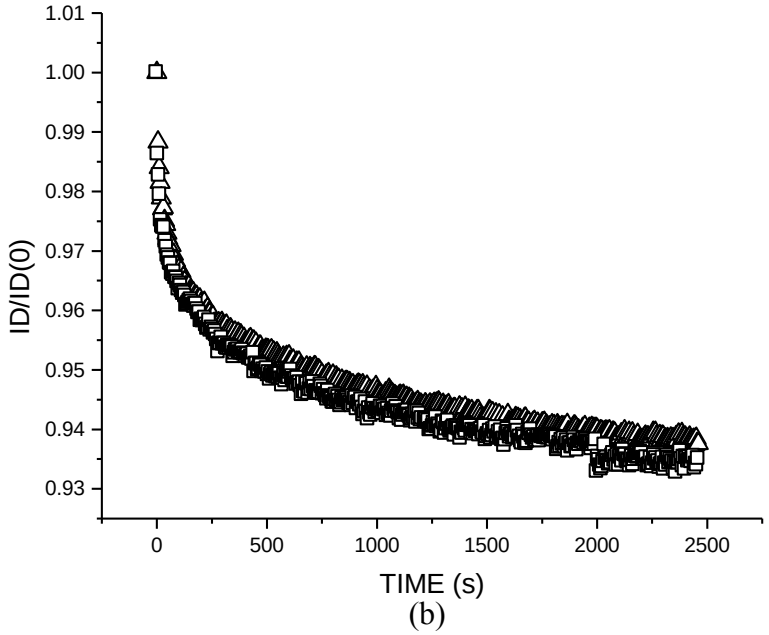


Figure 4-6) HfSiON threshold voltage shifts with time at T=175C and V_{gs} = -2.0V (Δ), V_{gs} = -1.7V (◊), V_{gs} = -1.5V (□), and V_{gs} = -1.3V (O). The curves can be fitted to the formula $\Delta V_{th}=At^{\alpha}$. The fitted parameters A and α are shown in TABLE 4-2.

The next challenge was to examine the behavior under different electric fields in the lateral sense. Fortunately we had the luxury of many different technology nodes on our HfSiON wafers. This enabled our first experiment which was to increase the device channel length from 1μm to 10μm without increasing the drain voltage. Consequently, the lateral electric field across the inversion channel, and the source-drain current were reduced by an order of magnitude. There was no correlation to a change in threshold voltage as seen in FIG 4-7 evidencing the fact that the physical mechanisms responsible for NBTI are unaffected by the magnitude of the source-drain current, length of the channel, or the lateral electric field. In hindsight, this result was not as surprising as initially thought, given that the effect is believed to be a result of the creation of interface states compounded with a faster hole trapping mechanism; neither of which should be constrained by the density of charge in the inversion channel or the electric field in the lateral sense.



(a)



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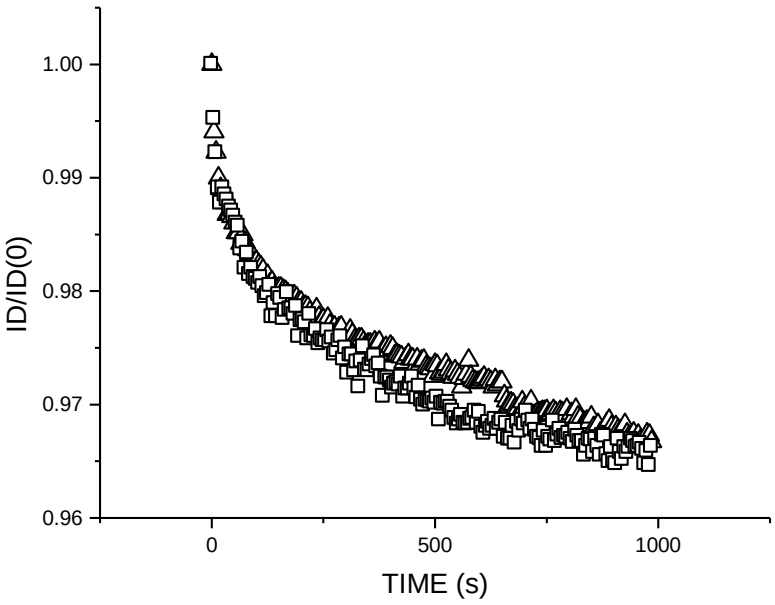


(c)

Figure 4-7) Ratio of the source-drain current to the initial source-drain current at t=0 for 10μm (Δ) and 1μm (□) technology nodes at bias voltage of a) -2.0V, b) -1.7V, and c) -1.3V

For completion, we performed At^{α} fits to the 1μm and 10μm data and compared the fitting parameters A and α. Examination of TABLE 4-2 confirms that over the range of bias voltages we selected, threshold voltage shifts are neither time nor magnitude dependent on the magnitude of the source-drain current; however, the same conclusion could not be drawn for their relative dependencies on the lateral electric field. This was the result of an unexpected enhancement in the magnitude of the threshold voltage degradation dependent on the level of the source drain voltage. Adjusting V_{ds} modifies the electric field in the lateral sense, as does increasing the channel length; however, the two experiments resolved completely different results. It is important to note that we repeated these results many times. Accordingly, in Chapter 5 we take a very serious look as to what the physical explanation for this enhancement could be. The details of the experiments that formed this curiosity are in the subsequent section.

V_{gs} (V)	$A_{10\mu m}$	$A_{1\mu m}$	$\alpha_{10\mu m}$	$\alpha_{1\mu m}$
-2.0	-0.0133	-0.0143	0.18	.18
-1.7	-0.0084	-0.0092	0.20	.19
-1.5	-0.0044	-0.0052	0.23	.22
-1.3	-0.0020	-0.0021	0.28	.28

Table 4-2) Fitting parameters A and α from continuous current measurements at 4 unique gate voltages on p-channel MOSFETs with 10μm and 1μm channel lengths. V_{ds} was -2.0V in all cases.

4.6 Linear Region Vs Saturation Region Stress Conditions

Experimentally, NBTI is usually examined by stressing the device with a chosen V_{gs} and maintain $V_{ds} = V_{body} = 0V$. This ensures a uniform vertical field, E_z, and a zero lateral field, E_x. To our knowledge, no model has predicted a threshold voltage dependence on the source-drain voltage directly related to the NBTI phenomenon [8, 9, 10, 11]. Indeed, it has been shown that devices with pure SiO_2 gate oxides exhibit no dependence on the V_{ds}. We did however consider it necessary to verify that this was consistent with our devices based on the HfSiON dielectric. Therefore, we developed an experiment to probe the dependence on V_{ds} over a wide range of voltages. All devices in these experiments were stressed with -2.0V on the gate and at a temperature of 175C. V_{ds} took the values -2.0V, -1.7V, -1.5V, -1.25V, -1.0V, -0.75V, -0.5V, -0.25V, and -0.1V. As a result, operational regimes of the devices shifted from the saturation region to the linear regime; consequently, it is necessary to use EQ 4-10 when interpreting continuous current measurements because this equation is valid over all modes of transistor operation.

Surprisingly, we observe a significant V_{ds} dependence that manifests itself as a dramatic decrease in ΔV_{th} as the device is biased at higher V_{ds}. This is clear in FIG 4-8 where we show $\Delta V_{th}(t)$ for a variety of V_{ds} values. For a device in the linear region (open squares, $V_{ds} = -0.1V$), we calculate a ΔV_{th} of 87.5mV after t = 630s. Keeping stress conditions the same with the exception of V_{ds}, a device in the saturation region (crosses, $V_{ds} = -2.0V$) shows ΔV_{th} of 21.6mV at t = 630s. At 175 ^{o}C after 700 s stress time, we typically see around 4x reduction in $\Delta V_{th}(t)$ for a measurement in saturation, as compared to those in the linear region. A profile of a range of V_{ds} values shows a systematic

decrease in $\Delta V_{th}(t)$ with increasing V_{ds} that appears to "saturate" as V_{ds} approaches -2.0 V.

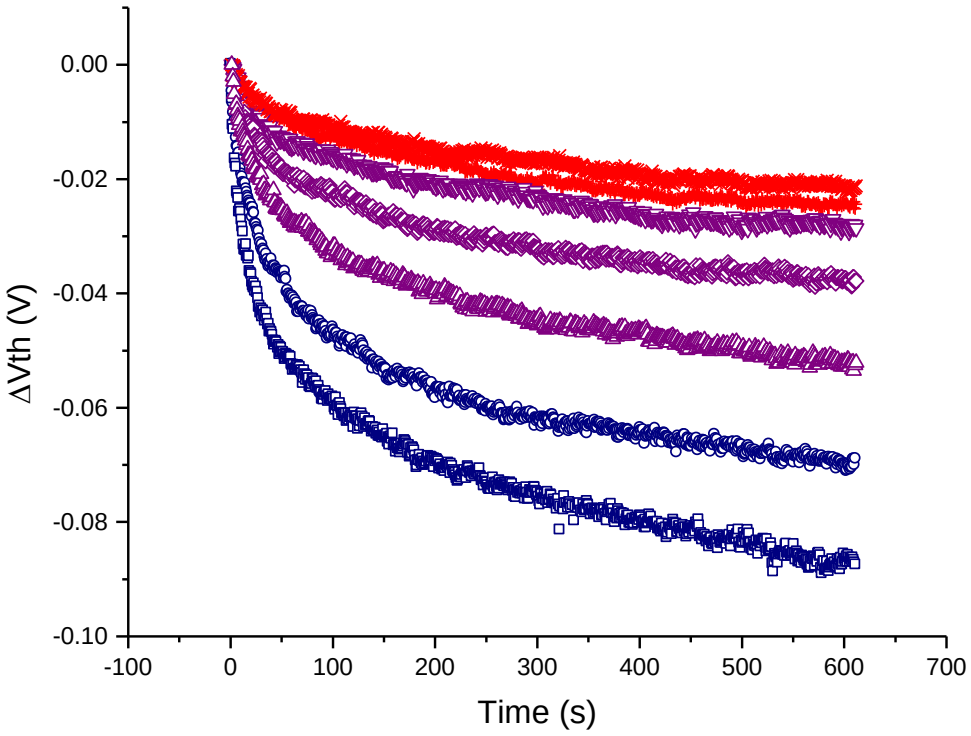


Figure 4-8) Threshold Voltage Shifts as a function of time and V_{ds} in HfSiON. (□) V_{ds} = -0.1V, (O) V_{ds} = -0.5V, (Δ) V_{ds} = -0.75V, (◊) V_{ds} = -1.0V, (▽) V_{ds} = -1.25V, (+) V_{ds} = -1.5V, (X) V_{ds} = -2.0V

In previous experiments we used At^{α} curve fits to deduce information of the time dependence associated with the $\Delta V_{th}(t)$ plots. In a new approach we take the ratio of each $\Delta V_{th}(t, V_{ds})$ with respect to the measurement $\Delta V_{th}(t,V_{ds}$ = - 0.1 V). For the case that two different curves exhibit identical time dependence the resulting ratio $\Delta V_{th}(t,V_{ds})$ /$\Delta V_{th}(t,V_{ds}$ = - 0.1 V) should be constant. Clearly there is a time dependence in the ratio shown in FIG 4-9. Confirming our suspicions of variable time dependence confined to

the early time domain is the fact that after several hundred seconds the ratio is roughly constant.

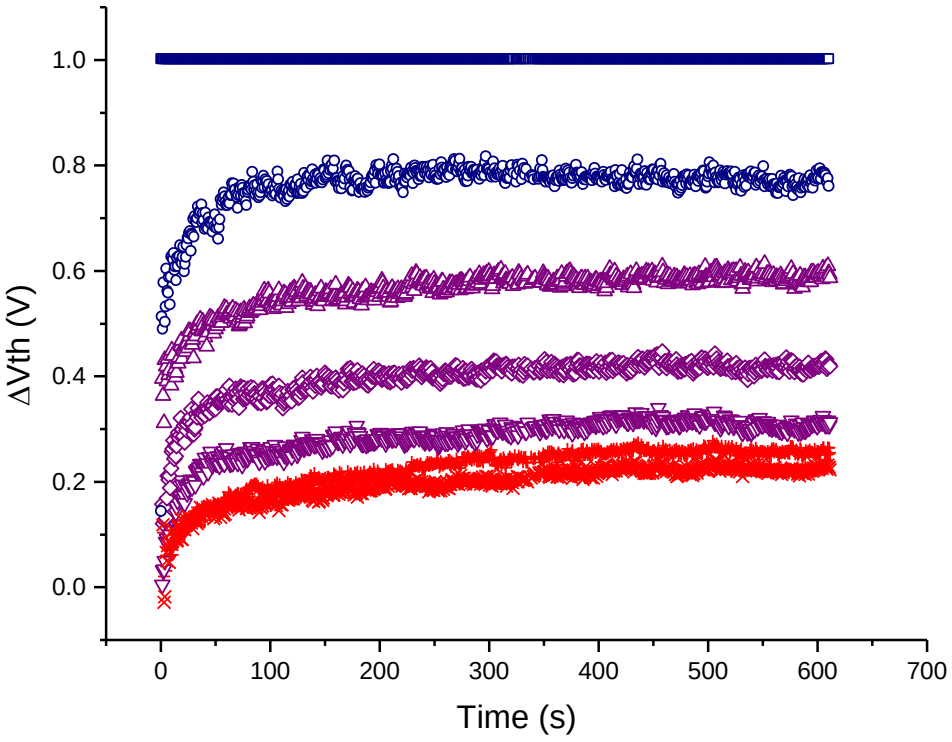
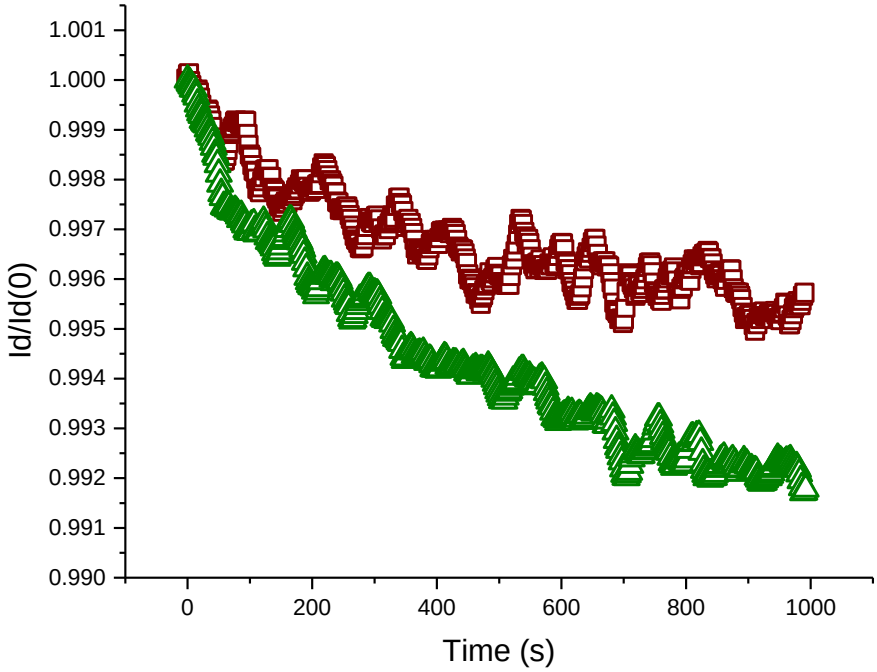


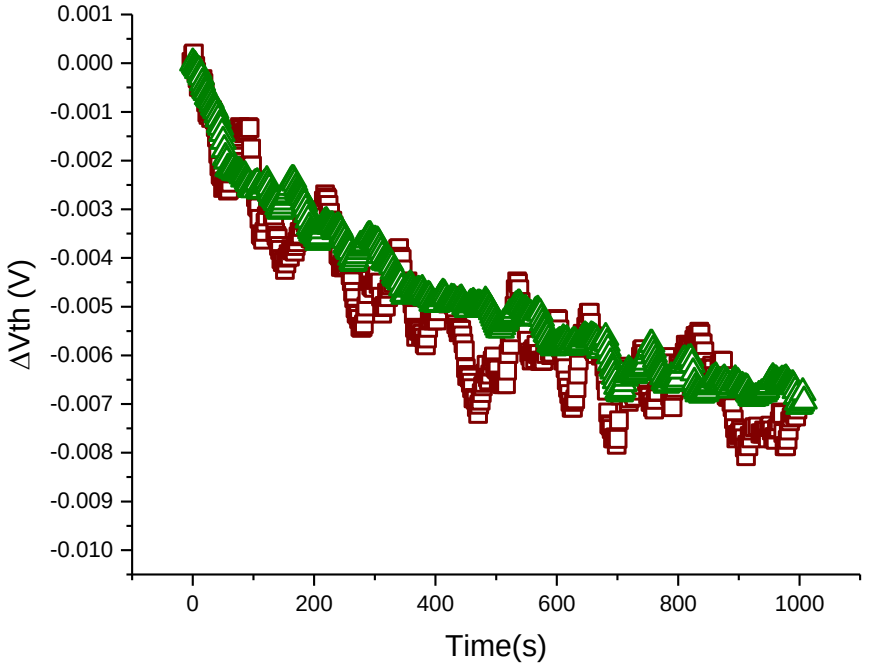
Figure 4-9) Ratio of $\Delta V_{th}(t, V_{ds})/ \Delta V_{th}(t, V_{ds}=-0.1V)$ in HfSiON. (□) V_{ds} = -0.1V, (O) V_{ds} = -0.5V, (Δ) V_{ds} = -0.75V, (◊) V_{ds} = -1.0V, (▽) V_{ds} = -1.25V, (+) V_{ds} = -1.5V, (X) V_{ds} = -2.0V

Given the unexpected/surprising results of our HfSiON experiments, we were compelled to verify that this was indeed a true effect and not a fabrication of our measurement technique or data analysis methodology. To do this we needed to verify that our SiO_2 samples behaved as expected [11]. That is to say we needed to show that the surprising enhancement of V_{th} as a function of V_{ds} was not present. In fact, examination of the square law model in EQ 1-1 tells us that ideally, for a given ΔV_{th}, the normalized

change in drain current $\Delta I_{ds}/I_{ds}^{o}$ measured in the saturation region should be twice as big as that in the linear region. Clearly this was not the case of the high-κ devices. As for the SiO_2 technology, we first examined the devices from Lincoln Labs at MIT.

Bias stress experiments were performed on MIT"s SOI substrate SiO_2 p-channel MOSFETs at a temperature of 195C. We elected to use 195C over 175C to maximize V_{th} degradation and improve our signal to noise ratio. A bias voltage of -2.0V was applied to the gate. V_{ds} took the values of -2.0V and -0.2V corresponding to saturation and linear regions respectively. Encouragingly, FIG 4-10 confirmed that our methods could consistently reproduce the expected results on SiO_2 technology. In this case the ratio of the drain current change for the devices stressed in the linear region (red squares) and saturation region (blue triangles) was approximately 2 at 1000s corresponding to a direct overlay of ΔV_{th} in linear and in saturation as shown by FIG 4-10b. Furthermore, by examining the curvature of $\Delta V_{th}(t)$ in FIG 4-10 it is clear that the NBTI effects in these devices are much smaller than those of HfSiON.

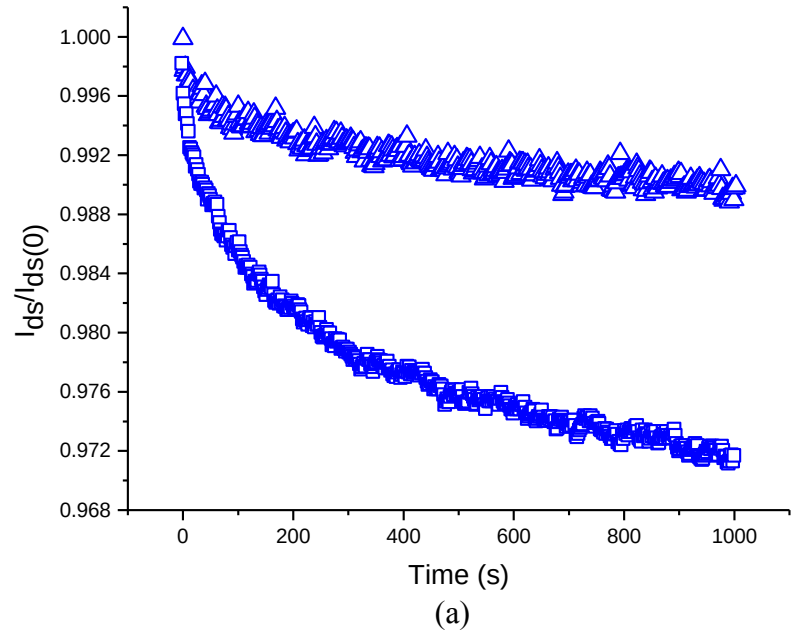




(b)

Figure 4-10) a) $\Delta I_{ds}(t) / I_{ds}^{o}$ for SiO_2 gate p-channel MOSFETs at 195 °C. Measurements were made in the linear regime (□) and saturation regime (Δ) b) Data converted to $\Delta V_{th}(t)$ using EQ 4-10. In both cases the gate-source voltage was maintained at -2V.

To further explore or understanding of how the effect of NBTI is manifest on different devices, we elected to perform continuous stress measurements on an additional set of SiO_2 devices from IBM‟s bulk Si 130nm technology. These experiments were performed at a temperature of 175C and a gate bias voltage of -1.8V. To facilitate transition from the saturation region to the linear region, experiments were executed with V_{ds} = -1.8V (saturation) or V_{ds}= -0.1V (linear). Illustrated by FIG 4-11 is the ratio of the normalized current measurements for the devices stressed in the linear region compared to the saturation region, the ratio is ~2.5; not perfectly consistent with previous results on the MIT SiO_2 samples. Apparently there is a different effect here acting in the opposite direction of that previously observed which appears to slow down the degradation of the devices stressed in the linear regime. The overlaying black curves in FIG 4-11b are the result of a second test verifying the consistency of this result. Though unexpected, the outcome of this experiment is not detrimental to the overall experimental methodology. Rather, these results emphasize the complexity relative or the mechanisms involved in NBTI as they relate to the device specifications.



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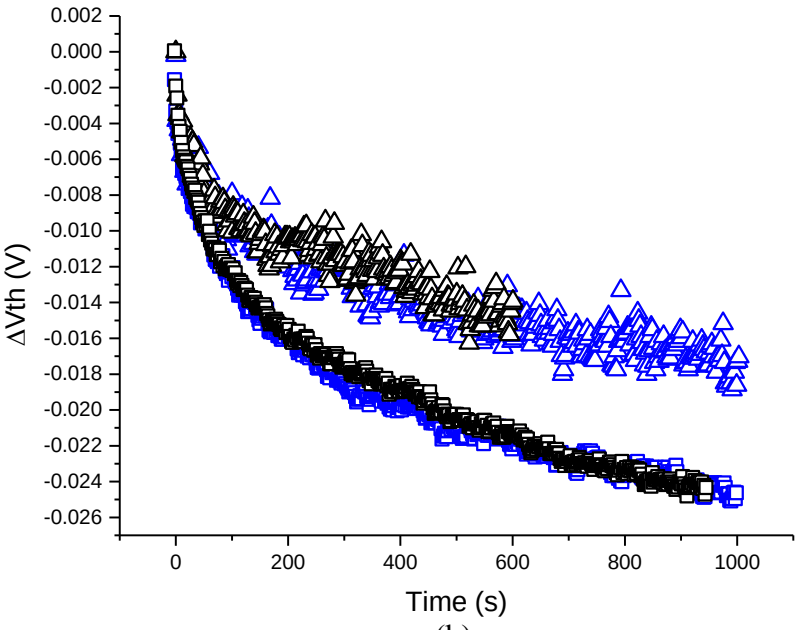

(b)

Figure 4-11) a) $I_{ds}(t)/I_{ds}^{o}$ results from IBM 130nm SiO_2 technology. Devices were stressed in the linear regime (Δ) and saturation regime (□) b) Data converted to $\Delta V_{th}(t)$ using EQ 4-10. Blackened data is result of an identical test performed on a different device. In both cases the gate-source voltage was maintained at -2V and T=175C.

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5. Chapter 5 – Discussion

The results of the experiments discussed in chapter 4 revealed many complexities involved with developing a physical model for the effects observed in NBTI. Clearly, previous attempts [1] have not been able to explain the time dependence observed in both HfSiON and SiO_2, nor the surprising enhancement of V_{th} degradation for devices stressed in the linear regime. Nevertheless, we have successfully extracted valuable information relative to the physical mechanisms at hand. Our final objective for this thesis was to discuss potential explanations for the effects that we have observed. Accordingly, we have been able to construct some interesting ideas, which could explain the origin of these effects. In this chapter we will discuss positive charge trapping kinetics and our lateral charge transport hypothesis.

5.2 Positive Charge Trapping Kinetics

The mechanisms of NBTI remain a mystery although it is widely accepted to be related to the trapping of positive charge/charged species at the dielectric/semiconductor interface or in the gate dielectric. The results in Chapter 4 have made it clear that a generic model is unlikely to accurately predict threshold voltage degradation among a variety of different technology specifications. This makes the issue of calculating the reliability lifetime of a circuit extremely complicated. We do not completely understand the underlying physics behind this effect; however, our experiments have exposed some critical results related to the charge trapping/relaxing behavior under a variety of different conditions

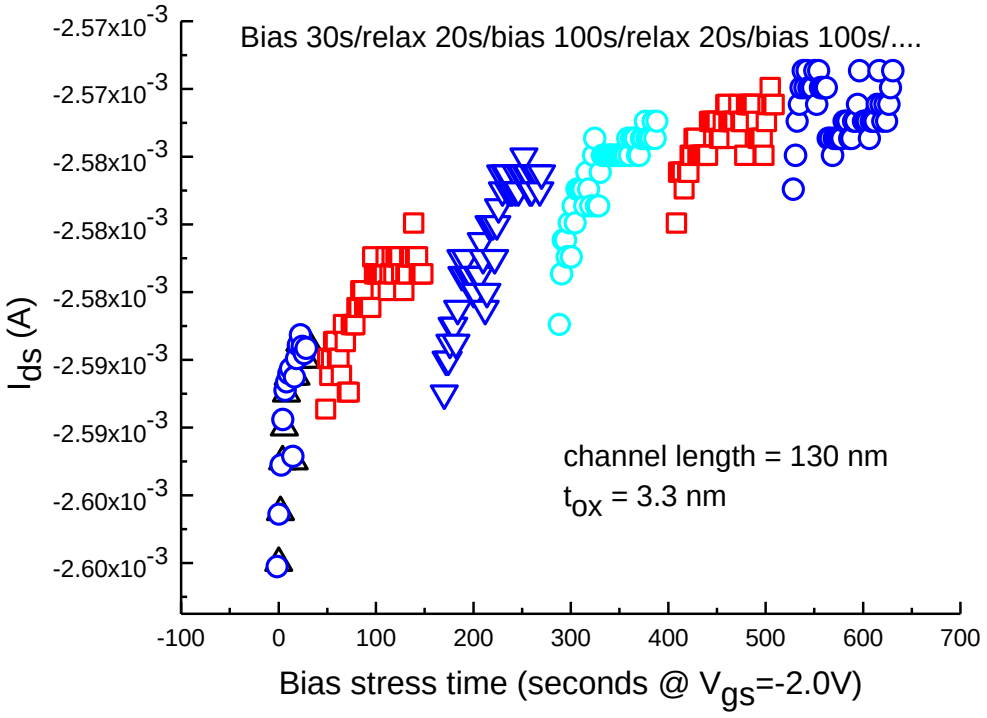
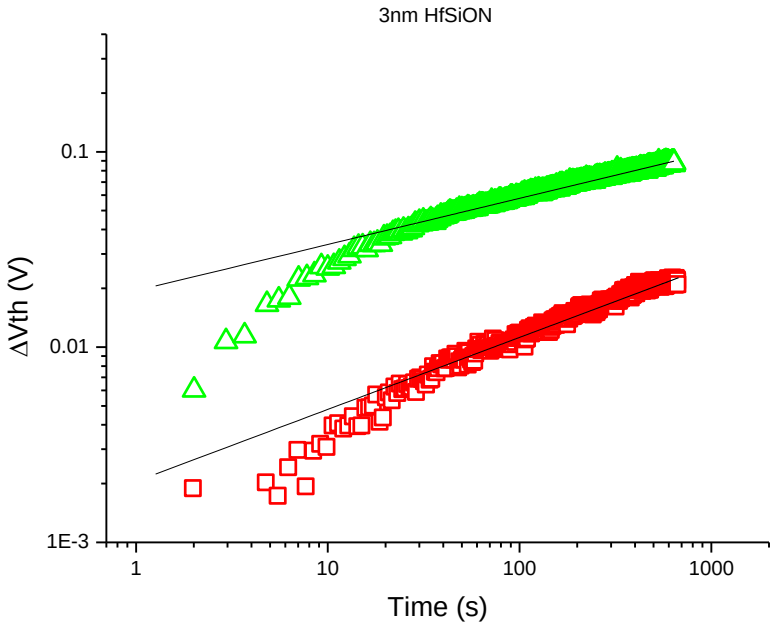


Figure 5-1) Charging/relaxing of charge 130nm SiO_2 showing the. The devices was biased for 30s / relaxed for 20s / bias 100s / relax 20s / bias 100s…

In FIG 5-1 we show the results of an experiment which involved applying a stressing bias to the gate for 100s, removing the stress for 20s, and then repeating. Clearly a substantial amount of the trapped charge is being released in the 20s of down time between stresses; however, a general trend upwards evidences the creation of a much slower, possibly permanent, effect. Speculation surrounding the origin of the positive charge induced by NBTI has evolved over time. As discussed in Chapter 2, initially NBTI was believed to be the consequence of a single mechanism which involved the release of neutral atomic H from passivated dopant species, followed by hole trapping from the inversion layer ($H + h^+ \rightarrow H^+$). The resultant proton, in the presence of an electric field, subsequently drifts into the bulk of the gate dielectric where trapping

occurs. It was believed that this mechanism would have a t^{α} time dependence [1] where α was ~1/6, corresponding to the time dependence of H^{+} electric field assisted drift [1]. However, experimental results were shown to deviate from the theory, specifically it could not adequately explain the recovery dynamics shown in FIG 5-1. Additionally, the notion of a t^{α} type time dependence has been shown to diverge from experimental results in the early time domain. Consequently, the concept of a two component charging mechanism has become the primary focus for our discussion.



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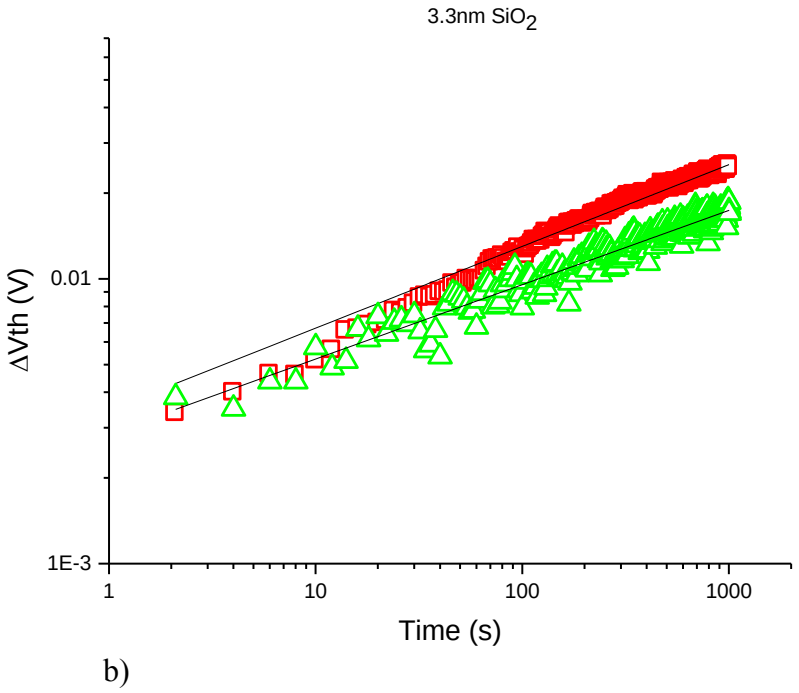


Figure 5-2) a) $\Delta V_{th}(t)$ on 3nm HfSiON devices biased in the linear regime (Δ) and the saturation region(□). b) $\Delta V_{th}(t)$ on 3.3nm SiO_2 devices biased in the linear regime (Δ) and the saturation region(□). Solid black lines represent At^{α} fits.

The behavior at long time is reasonably consistent among all the different device technologies we have studied. In almost all cases, an initial rapid charging mechanism was constrained to the early time domain, ultimately overtaken by a secondary mechanism which we now believe to be the creation of interface states. The interface states are believed to be stable so the recovery dynamics must be explained by the relaxation of charged defect sites in the oxide. Understanding the physics of the initial charging mechanism and the charge relaxation effect has been complicated by the disparity of threshold voltage degradation between the different device specifications.

It may be possible that the initial mechanism involves the rapid charging of defect sites near the semiconductor/insulator interface. The charged species would be holes from the inversion channel. The question still remains as to how the holes enter the oxide; it

could be related to a tunneling mechanism similar to Fowler-Nordheim tunneling [2]. In any event, experimental results have shown that this mechanism does not show simple power law time dependence [3]. This is apparent in FIG 5-2a where we show ΔV_{th} on a HfSiON transistor stressed in the linear regime (green triangles) and the saturation region (red squares) with the solid black lines showing the power law fits to the data. Intriguingly, the high-κ device displays considerably more deviation from the t^{α} time dependence than the standard SiO_2 devices, FIG 5-3b. This is evidence of an initial rapid charging mechanism which is predominate in the HfSiON samples but reduced in the SiO_2 devices presumably due to the low density of defects at the Si/SiO_2 interface. Curiously, examination of FIG 5-1 reveals that charge relaxation is still evident in SiO_2 raising question about the relationship between the initial charging and relaxation mechanisms.

5.2 Lateral Charge Transport Theory

In our experiments we found changes in threshold voltage induced by NBTI on p-channel MOSFETs with HfSiON gate dielectrics to be a function of the source-drain voltage. This effect manifests itself as an enhancement in V_{th} degradation when stressing a device in the linear regime. To our knowledge this is not anticipated by any previous models [3,4,5,6]. For comparison/verification we examined the equivalent effect on two sets of devices with SiO_2 gate dielectric. Encouraging, these experiments revealed that the anomaly was not present either sample of SiO_2. In one of the SiO_2 samples we did reveal what appeared to be a small V_{th} dependence on V_{ds}; however, the magnitude and

direction of these shifts suggest the mechanisms are different than those creating V_{ds} dependence in HfSiON.

As discussed in Chapter 4, some uncertainty may arise in our data interpretation methodology because of the difficulty in obtaining I_{ds}^{o} which leads to potential error in the $\Delta I_{ds}/I_{ds}^{o}$ estimation. To confirm our initial conclusions regarding modifications of V_{th} degradation base on the mode of operation, an alternative approach is used, which involves analysis of the time derivative of the square law model for both saturation and linear regions. Beginning with the basic square law in EQ 1-1, we define $k \equiv (W/L)\ \mu_{eff}\ C_{ox}$. Next, for the case of the saturation analysis we set $V_{ds} = V_{gs}-V_{th}$ which gives us the following expression:

$$I_{ds}|^{sat} = k/2\ (V_{gs}-V_{th})^2 \tag{5-1}$$

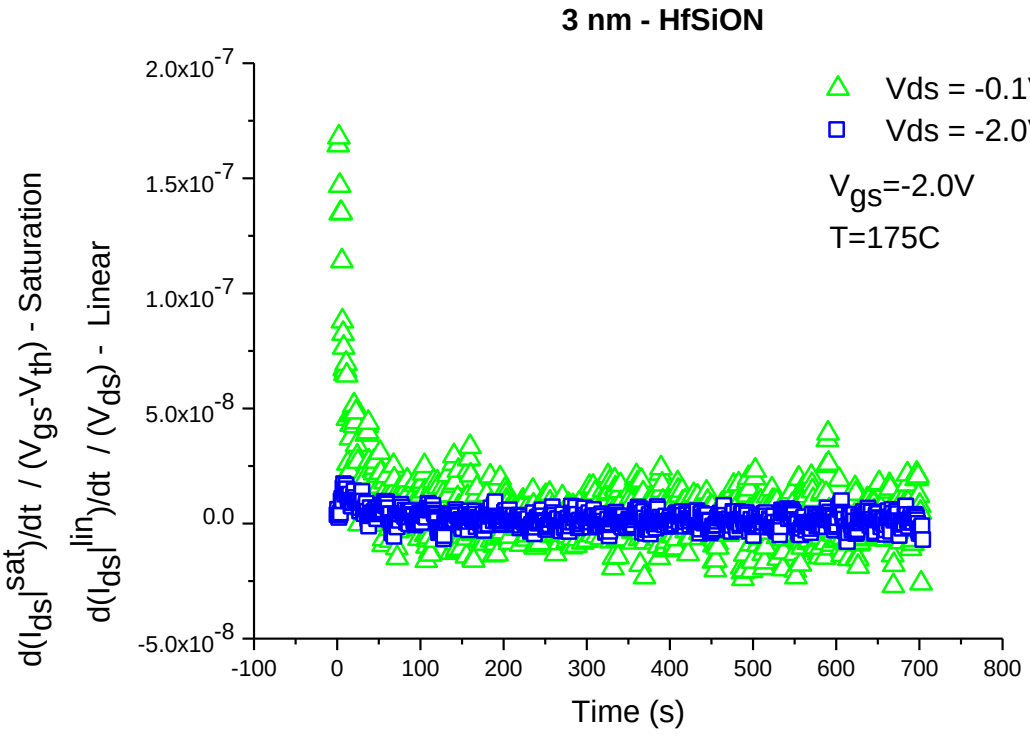
Taking the derivative with respect to time of EQ 5-1 then rearranging we get:

$$k*d(V_{th})/dt = (\ d(I_{ds}|^{sat})/dt\ ) / (V_{gs}-V_{th}) \tag{5-2}$$

Subsequently, the same analysis must be performed for the case of the linear regime. It can easily be shown that the time derivative of the linear source-drain current law yields:

$$k*d(V_{th})/dt = (\ d(I_{ds}|^{lin})/dt\ ) / (V_{ds}) \tag{5-3}$$

Recall that we have performed continuous source-drain current measurements on devices stressing in both, saturation and linear modes of operation. Using software tools, we can take the time derivative of these continuous current measurements. Accordingly, plots of the right-hand-side of EQ 5-2 for $I_{ds}|^{sat}(t)$, and the right-hand-side of EQ 5-3 for $I_{ds}|^{lin}(t)$, as a function of time should yield identical curves. Note that analysis is less approximate than that of EQ 4-10 because it does not require an initial source-drain current measurement I_{ds}^{o}.



(a)

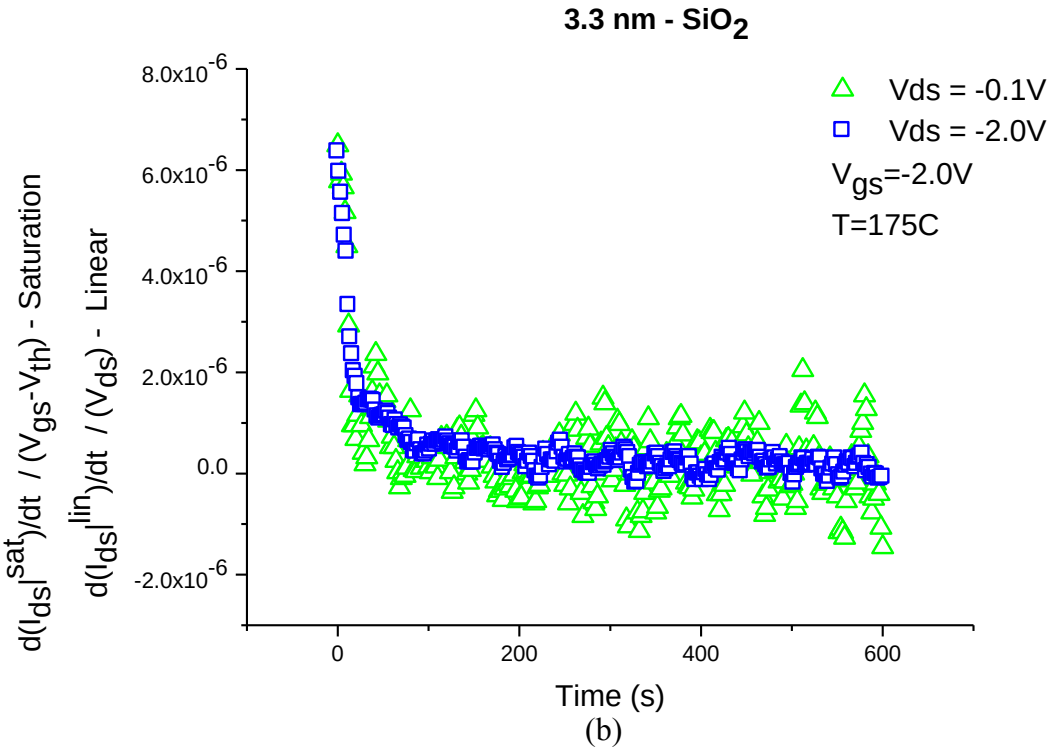


Figure 5-3) $d(I_{ds}|^{lin})/dt$) / (V_{ds}), and ($d(I_{ds}|^{sat})/dt$) / (V_{gs}-V_{th}) as a function of time for devices operating in the linear (Δ) and saturation (□) regime on a) HfSiON, and b) SiO_2 gate dielectrics.

In FIG 5-3 we display the results of $d(I_{ds}|^{lin})/dt$) / (V_{ds}), and ($d(I_{ds}|^{sat})/dt$) / (V_{gs}-V_{th}) as a function of time for devices stressed in the linear (green triangles) and saturation (blue squares) regions. Details of the measurements were discussed in Chapter 4. FIG 5-3b reveals a very nice overlay of the two results in SiO_2 evidencing well behaved characteristics of these devices in both modes of operation. On the other hand, FIG 5-3a reveals that while HfSiON devices stressed in the linear region displayed similar curve shape to the well behaved SiO_2 samples, the devices stressed in the saturation region exhibited a significantly lower charge trapping rate in the early time domain. This analysis clearly reveals anomalous behavior associated with stressing in the saturation

mode. In particular, the mechanisms that result in rapid charge trapping in the early time domain on our SiO_2 devices (and HfSiON devices stressed in the linear region) are significantly suppressed when stressing these HfSiON devices in the saturation region. To determine the origin of this effect we explored several options.

The first explanation which comes to mind is a short-channel effect in which charge is created non-uniformly at the drain end. One might expect that a parameter which modifies the density of charge in the inversion channel would also modify the magnitude of ΔV_{th}; however, we have shown that NBTI is not constrained by the charge in the inversion channel. In addition, if short-channel effects were to blame we would expect to see the same results on SiO_2 devices, but we do not. Nevertheless, we felt compelled to make a stronger argument to completely rule out the possibility of short-channel effects, thus we elected to explore the magnitude of non-uniform charging in the channel via a quasi-two-dimensional model [7].

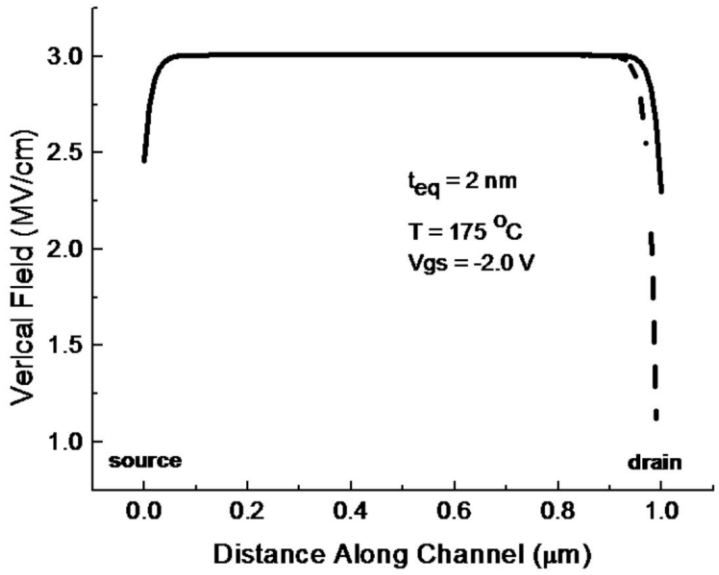


Figure 5-4) Vertical electric field $E_z(y)$ in the oxide as a function of distance along the channel obtained from a quasi-2D model of the surface potential. Solid line: V_{ds} = - 0.1 V; dashed line: V_{ds} = - 2.0 V.

The purpose of this model is to calculate the surface potential V_s along the channel length while accounting for 2D effects present near the drain and source contacts. We have applied the model to the geometry of our devices, using V_{bi} = 1 V, V_{FB} = 0, and V_{th}^{o} = -0.5 V, the oxide permittivity appropriate to SiO_2 with an oxide thickness t_{ox} of 2 nm, and semiconductor parameters at 175 ^{o}C. From the surface potential we have calculated the oxide field as a function of distance along the channel as $E_z(y) = [V_{gs} - V_s(y)] / t_{ox}$. A plot of $E_z(y)$ is shown in FIG 5-4 for the case of V_{ds} = -0.1 V and -2 V. FIG 5-4 confirms that regardless of the mode of transistor operation, our devices experience essentially a uniform $E_z(y)$ profile over nearly the entire channel length. Ultimately, given that the substrate doping densities were of the order of ~10^{18}, and the equivalent oxide thickness was ~2nm, it is to be expected that these devices behave "long-channel like".

We have shown that the vertical electric field is uniform across the entirety of the channel. However, that alone is not enough to exclude the possibility of non-uniform trap generation. It is possible that the non-uniformity of the vertical electric field is amplified by the generation rate resulting in significantly more charge in one case or another. The vertical electric field dependence of the charge generation rate $G(E_z)$ as a result of NBTI has been estimated by various authors to be of the form [8] $G(E_z) \sim E_z e^{\gamma E_z}$, where γ = 0.6. In FIG 5-5 we show the generation rate of charge as a function of distance along the channel. Again, this rate appears to be relatively uniform across the entirety of the channel. Consequently, we can conclude that the non-uniformity of the vertical electric field cannot explain the level of decreased trapped charge generation present in our devices stressed in the saturation region compared to the linear regime.

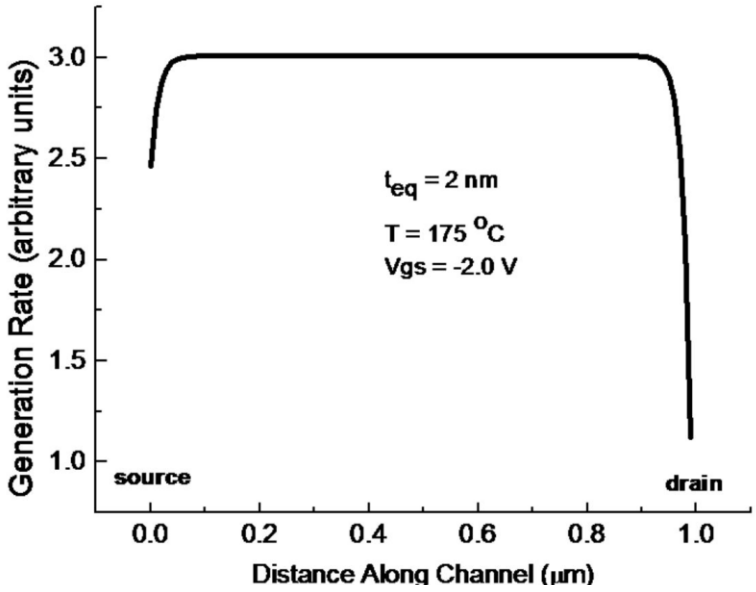


Figure 5-5) Generation of charge as a function of distance along the channel derived from the $E_z(y)$ calculations then translated the generation rate via the relation $G_z(y) \sim E_z e^{\gamma E_z}$

The exclusion of the possibility that short-channel effects are responsible for the linear versus saturation results in HfSiON has pressed us to explore alternative explanations for the phenomenon. NBTI produces a high density of positive charge near the semiconductor/insulator interface. We therefore hypothisize that given the complexities of the high-κ dielectric deposition, a SiON/HfSiON layer exists above the Si substrate. This mismatch interface contains a high defect density whereby positive charge is believed to be highly mobile in the lateral sense [9]. Lateral charge redistribution effects have been observed in other dielectric system such as in the SONOS memory cell [9,10]. We conclude that a previously unreported charge "leakage" mechanism exists in which trapped charge drifts through the high-k dielectric in a region of the dielectric parallel to the semiconductor/dielectric interface, and exits via the drain. This drift may be partially assisted by the electric field induced by V_{ds} [11] in the x direction in the oxide. Such trapped charge drift is absent in the case of devices with pure

SiO_2 gate dielectrics, because the density of defects in SiO_2 devices is significantly less than in high-κ materials and the interfaces are well defined. Furthermore, this hypothesis is supported by the fact that after a certain threshold of V_{ds} has been achieved, ΔV_{th} shift becomes almost independent of further increase in V_{ds} possibly because the probability of a charge escaping a potential well has maximized as the barrier height is lowered [12] by the V_{ds} related field. Though the underlying physics behind this lateral transport is not completely understood, this mechanism, or one similar, is to our knowledge the best explanation for the experimental results of this study. Beyond the scope of this thesis, we will continue to examine this effect and are optimistic that we will refine this theory.

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6. Chapter 6 – Conclusion

Negative Bias Temperature Instability (NBTI) has been recognized as a critical issue which may limit the reliability lifetime of space qualified electronics in future technology generations. When a p-channel MOSFET is subjected to elevated temperature and negative voltage bias with respect to the gate, we typically observe a decrease in source-drain current with time corresponding to an increase in threshold voltage. Given that the equivalent effect is not observed on n-channel devices, NBTI is believed to be a consequence of positive charge trapping in the gate dielectric possibly at the semiconductor/insulator interface.

Originally, the effect was believed to be explained by the Reaction Diffusion model, which claimed holes from the inversion channel could depassivate Si-H bonds, resulting in a proton (H^+) that in the presence of the external electric field would drift toward the gate. Further investigation proved that the issue was actually much more complicated. The first concern involved the measurement technique employed during data acquisition. RD theory was based on a stress/measure/stress protocol that has since been shown to be inadequate over early time regimes. This was evidenced by modern on-the-fly (OTF) techniques which had the ability to monitor threshold voltage shifts as a function of time without removing the stressing bias. OTF measurements revealed that stress/measure/stress methods severely underestimated the magnitude of the threshold voltages shifts because they did not account for charge relaxation during the I_{ds} acquisitions. In our experiments, we continually monitor the current while maintaining V_{bias}, then subsequently translate the ratio of $I_{ds}(t)/I_{ds}^{o}$ into a $\Delta V_{th}(t)$ plot. This method is not without approximation; however, we have been able to show both experimentally and

mathematically that our methodology is sound to first order. For the purpose of gaining an understanding the underlying physics associated with NBTI, we performed a number of experiments designed to explore the time and magnitude dependencies of the phenomenon on temperature, vertical electric field, charge density, and source-drain voltage. The corresponding experiments were executed on p-channel MOSFETs with an assortment of technology specifications to enhance our perception of the behavior of V_{th} shifts on a variety of gate dielectric compositions.

Initially we uncovered a large amount of information regarding the relevant dependence of V_{th} on temperature, vertical electric field, and charge density. The experimental data was captured using our own variant of an OTF measurement. The data analysis was accomplished using a traditional method in which we fit $\Delta V_{th}(t)$ curves to the power law, $\Delta V_{th} = At^{\alpha}$, then subsequently compared the fit parameters A and α. In doing this we revealed that the power law fit approach was a useful utility for comparing the "long time" behavior, but was not an accurate representation of the experimental data in the early time domain. This triggered the idea of a multi-mechanism process in which a rapid charging of defects in the dielectric takes place in the "short time" regime, and is ultimately overtaken by a slower but more permanent mechanism in the "long time" regime. We speculate that this long time process is due to the creation of interface states.

Continuing our investigation, we discovered a previously unreported dependency on V_{ds} which resulted in a reduction of V_{th} shifts when biased in the saturation regime during NBTI. Interestingly, this effect was observed on the HfSiON devices but not in the transistors with SiO_2 gate dielectric. To explain these observations, we initially explored the magnitude of non-uniform charging in the channel via a quasi-two-dimensional

model. Upon analysis of the model results, non-uniform charging was excluded as a possibility for this effect. Accordingly, we proposed an explanation for the effect wherein positive charge is laterally mobile at the SiON/HfSiON layer in the high-κ dielectric. In the presence of a finite vertical electric field induced by V_{ds}, the positive charge is partially swept out the drain contact reducing the initial rapid charging mechanism, thereby resulting in a reduction in V_{th} degradation.

In the future, we plan to continue the investigation of NBTI by introducing a new accessory to the Keithley 4200 SCS system which will enable the rapid acquisition of $I_{ds}(V_{gs})$ curves. More specifically we should be able to acquire a complete $I_{ds}(V_{gs})$ characteristic curve in under 100μs! In addition to the reduced level of approximation in data interpretation methodology, the ability to perform a "rapid IV" will facilitate our ability to probe the frequency spectrum of the charging/discharging kinetics associated with NBTI. Furthermore, the graphical user interface will enable us to generate an infinite variety of test waveforms opening the door to numerous experiments.

In conclusion, we have systematically achieved all 4 of our initial objectives. First, we reviewed traditional measurement techniques and data interpretation methodologies which ultimately gave way to our own optimized experimental procedure. Secondly, we performed a large variety of experiments on high-κ technologies and, thirdly compared the results to SiO_2 devices. Finally, we presented evidence of a two-component mechanism to explain the trap charging kinetics and proposed a lateral charge transport theory to explain the unusual reduction of V_{th} shifts in HfSiON MOSFETs when stressed in the saturation regime. In addition to our outlined objectives, our results have made it clear that the task of creating a reliable lifetime predictor formula is potentially

impractical due to the complexities discussed above. Undoubtedly, the need for a physical understanding of the mechanics involved is essential for the progression of a mathematical model. It is hoped that our experiments have shed some light on the nature of the physical phenomenon of NBTI, including valuable insight into the relevant variables.